

SPU

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REVISION HISTORY

REV	DATE	PAGES AFFECTED
D01	8/11/84	RELEASE SPU D TO MANUFACTURING
D08	8/11/84	SPU.2 CPU.4, 5, 8 AND SPU.2 CPU.4 RFC.1 AND SPU.2 DIAG.1, 2, 9 AND SPU.2 IO.3, 9 AND SPU.2 PBUS.3, 5

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DEFINITIONS
 CONVEX
 410-000131-300 D08

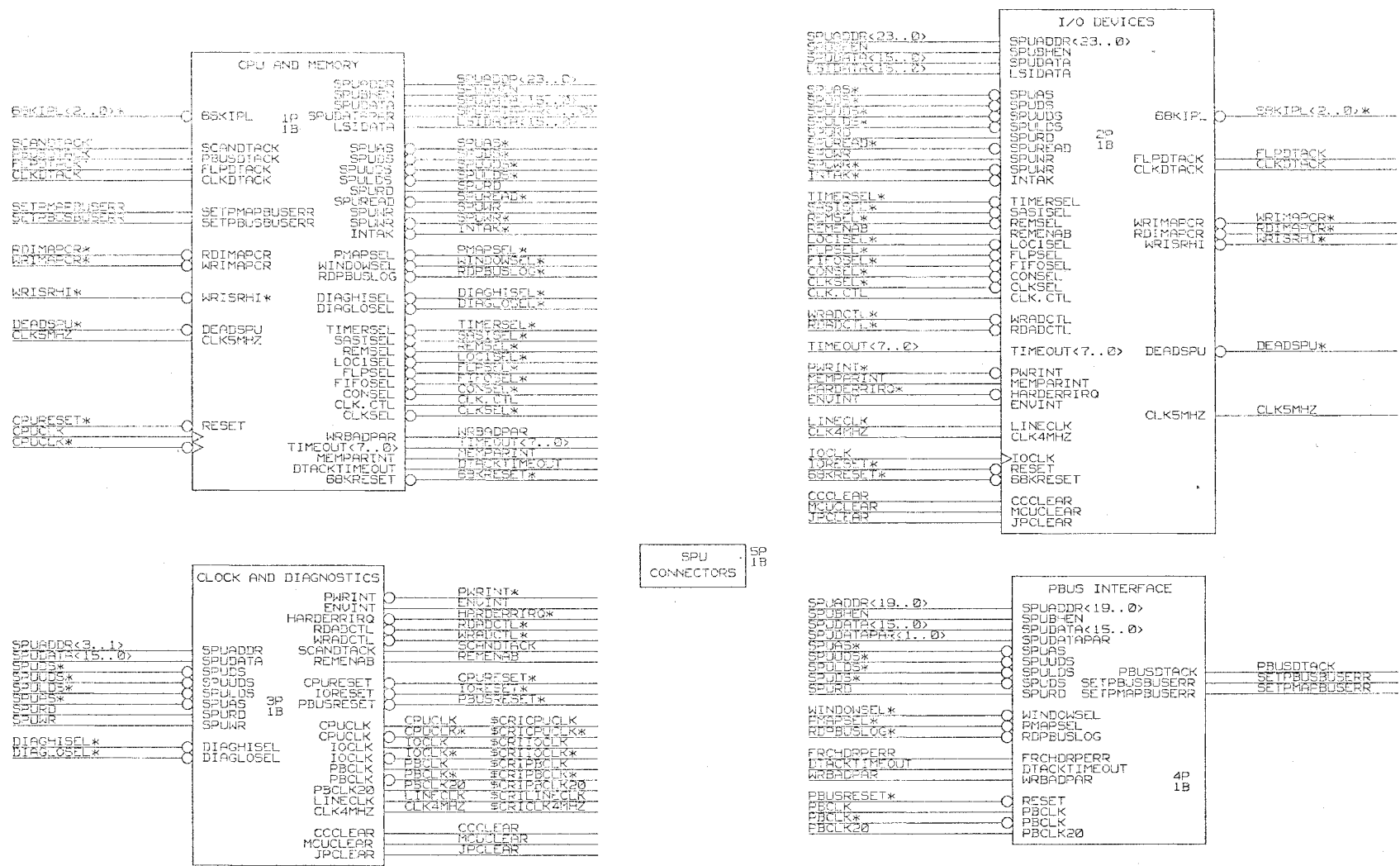


CONVEX

TITLE: SPU (COVER)
 DRAWING: 410-000131-300 D08

ABBR: SPU
 ENGR: NOBLES

REVISED: Mon Jan 7 10:53:16 1985 PAGE: SPU.1

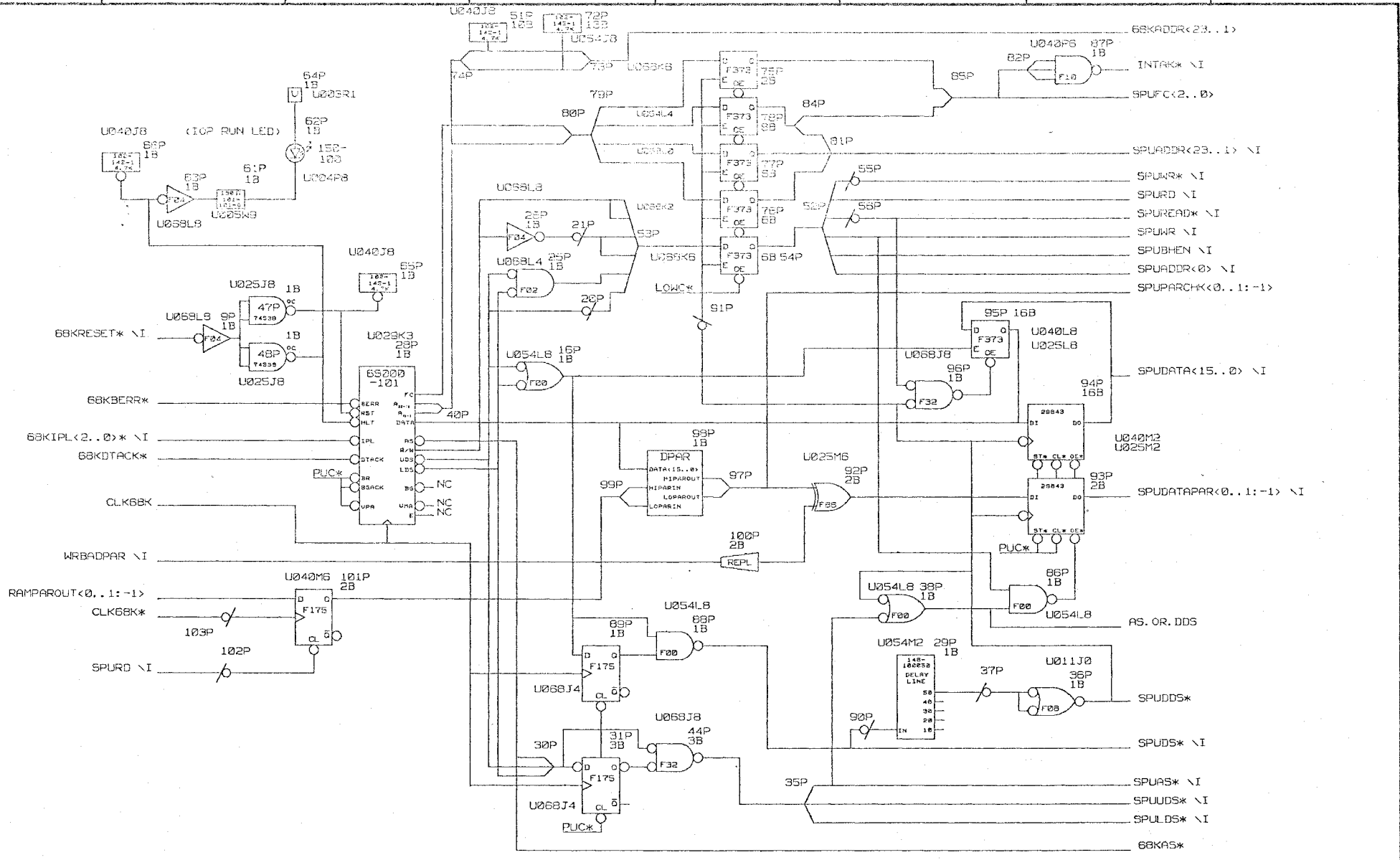


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TITLE: SPU
 DRAWING: 410-000131-300 D01
 REVISED: Fri Sep 14 10:59:59 1984
 ASBR: SPU
 ENGR: NOBLES
 PAGE: SPU.2

8 7 5 5 4 3 2 1



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DEFINE
XREFS
M.STYLE



CONVEX

TITLE: CPU (68K AND BUFFERS)

DRAWING: 410-00131-300 D01

REVISED: Tue Sep 11 10:55:44 1984

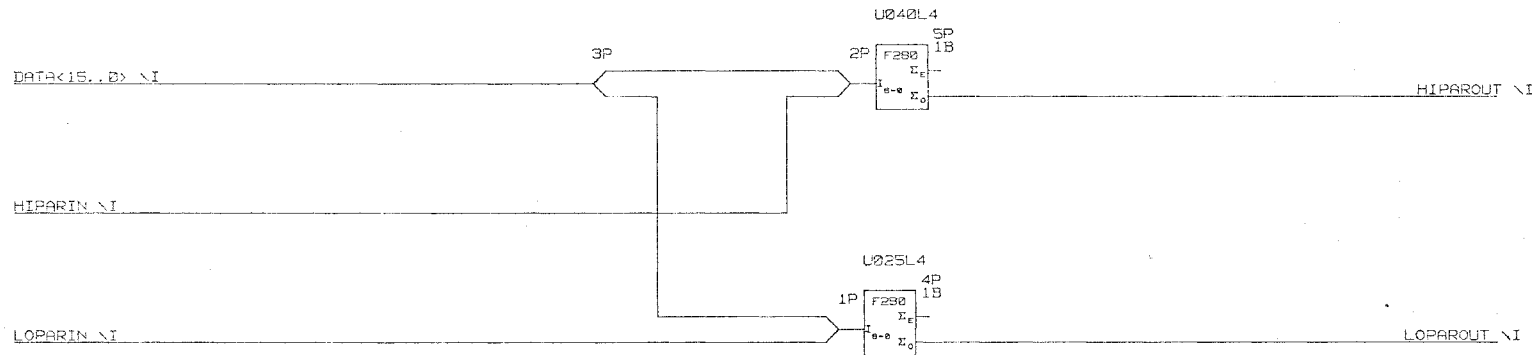
AB99: CPU

ENGR: NOBLES

PAGE:

SPU.2 CPU.1

8 7 5 5 4 3 2 1



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DEFINE
X-FIRE
K-STOPS

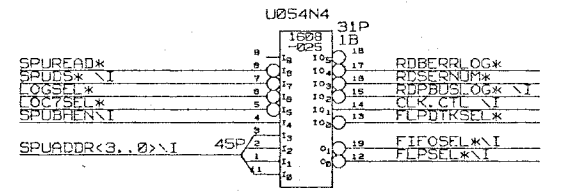
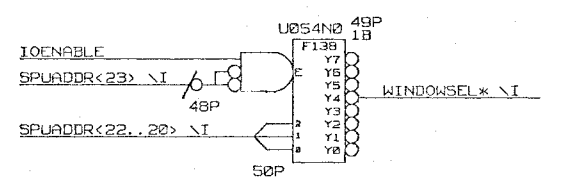
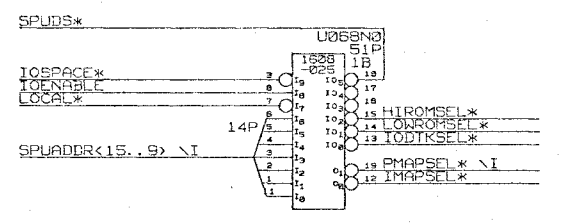
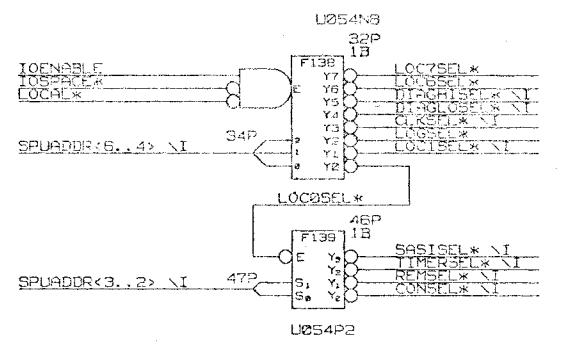
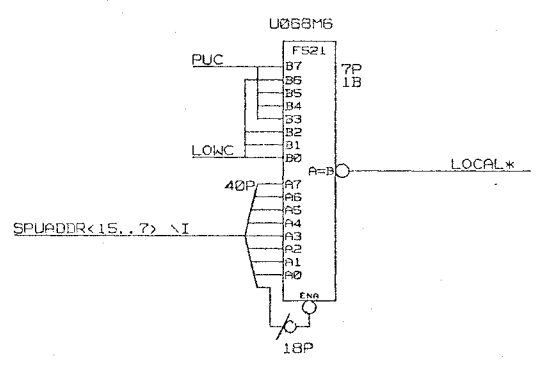
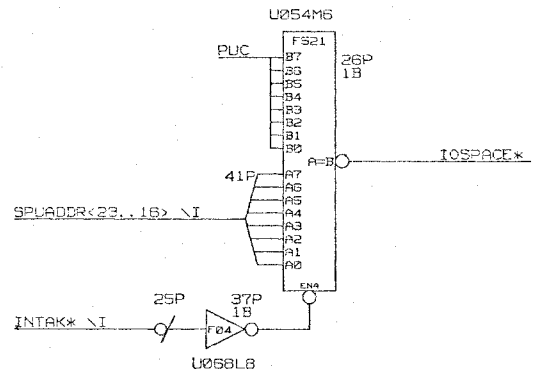
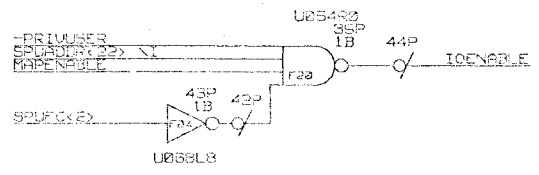


CONVEX

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DRAWING: 410-000131-300 D01

ABBR: DPAR
ENGR: LOCKHART

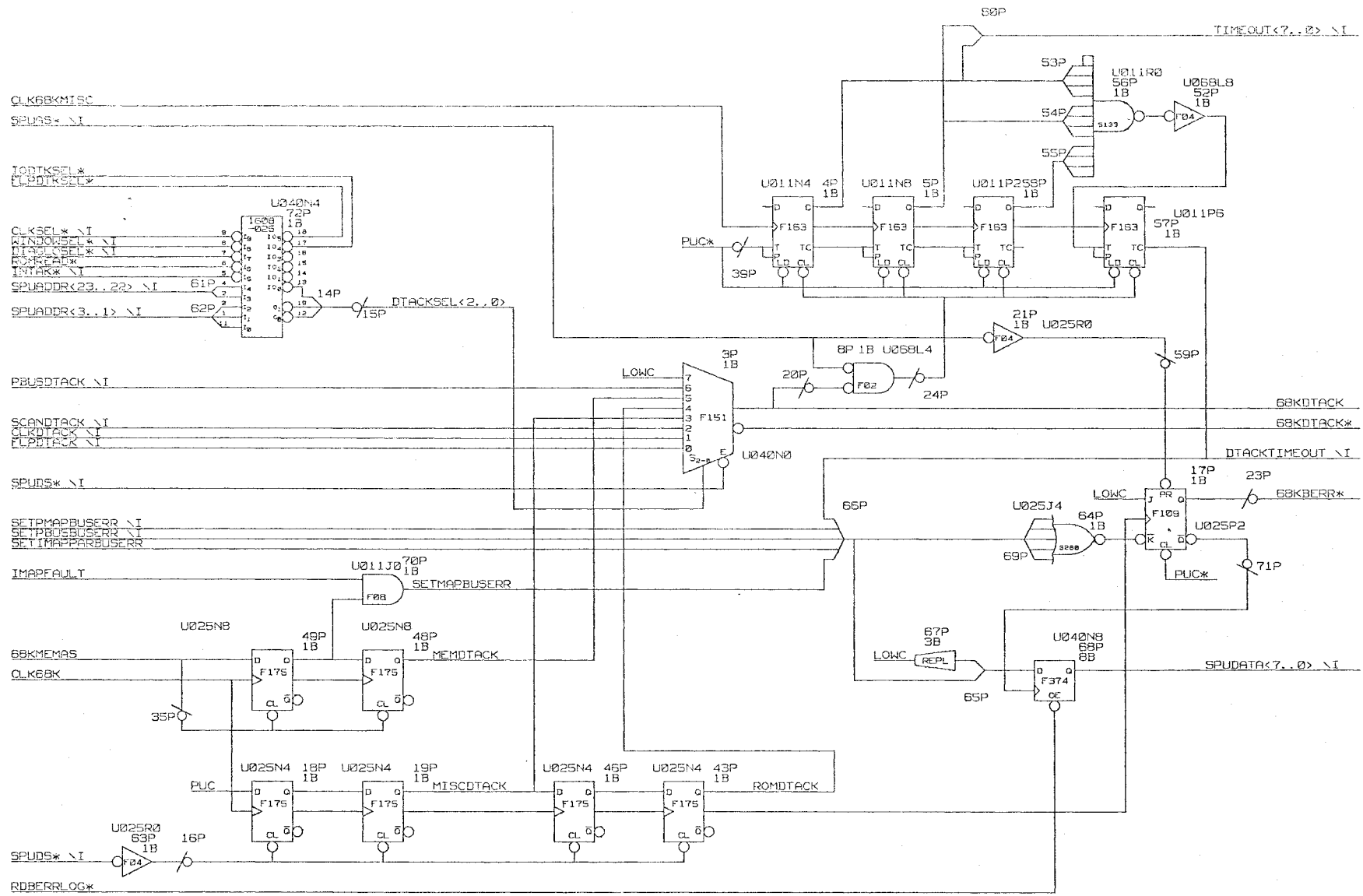
REVISED: Mon Sep 10 16:47:11 1984 PAGE: SPU, 2 CPU, 1 DPAR1



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TITLE: CPU (ADDRESS DECODE) ABBR: CPU
 DRAWING: 410-000131-300 D01 ENGR: NOBLES
 REVISED: Mon Sep 10 16:09:50 1984 PAGE: SPU.2 CPU.2



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TITLE: CPU (DTACK AND BUSERROR)

DRAWING: 410-000131-300 D01

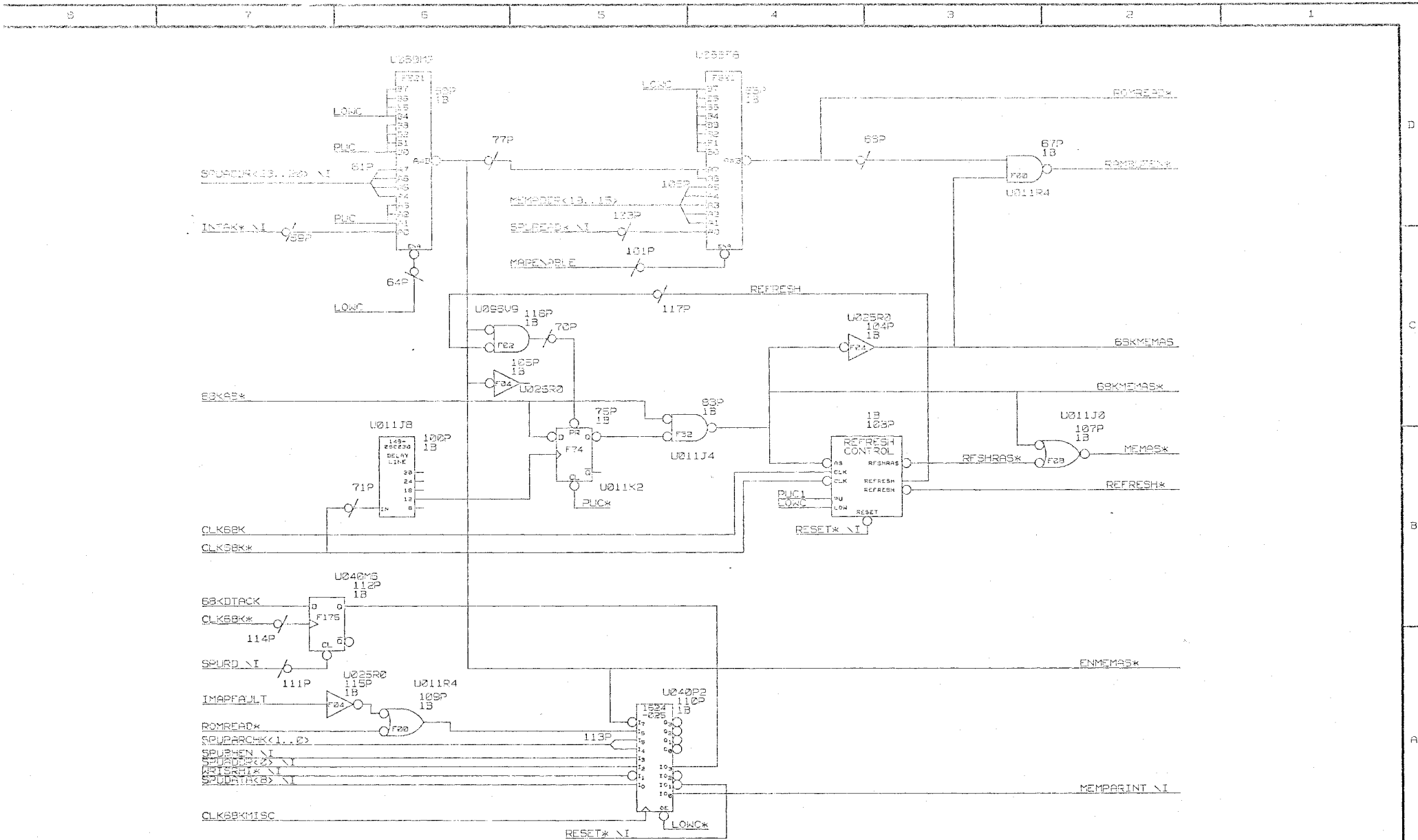
REVISED: Mon Sep 10 16:11:11 1984

ABBR: CPU

ENGR: NOBLES

PAGE:

SPU.2 CPU.3



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TITLE: CPU (MEMORY CONTROL)

ABBR: CPU

DRAWING: 410-000131-300 D08

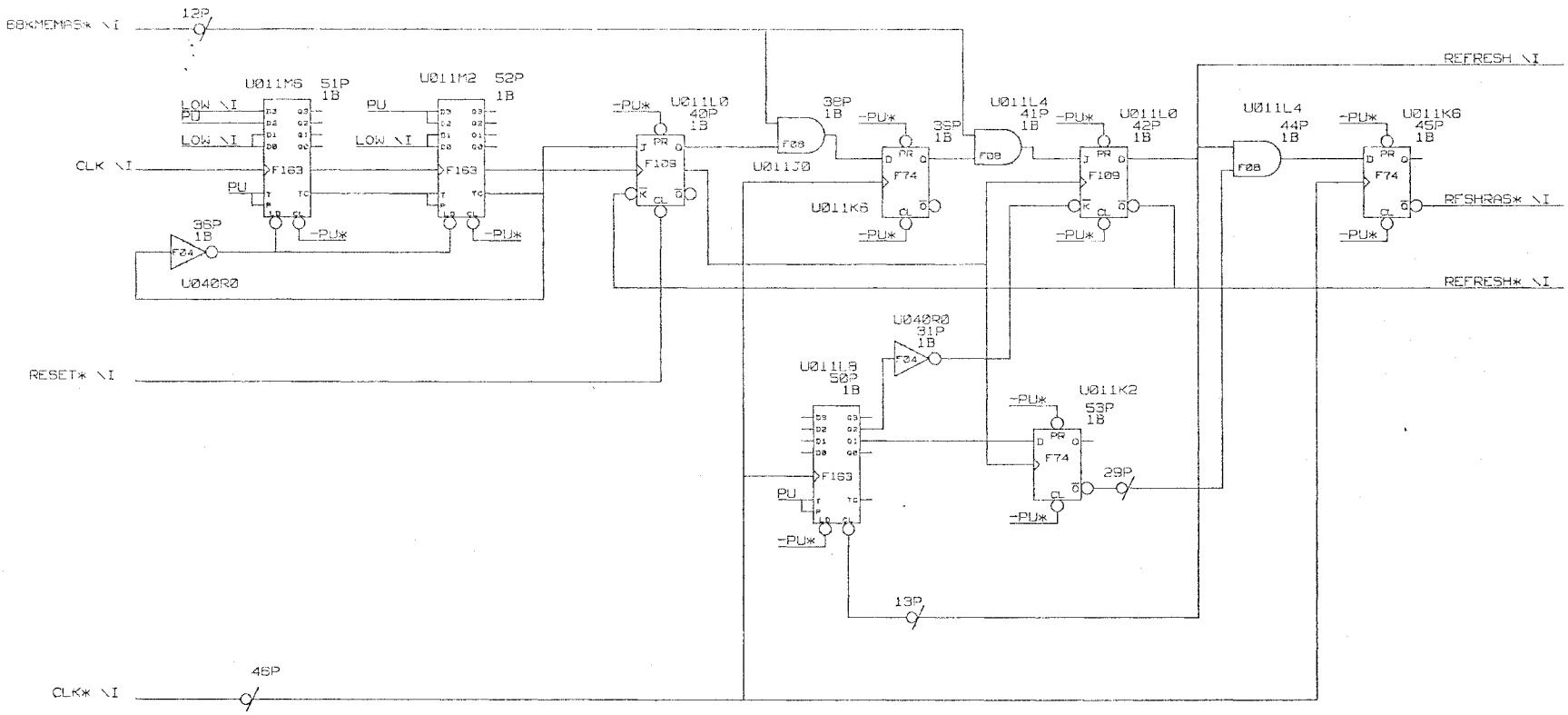
ENGR: NOBLES

REVISED: Fri Jan 4 11:06:44 1985 | PAGE:

SPU, 2 CPU, 4

REQ SYNC GRNT (RFSH) RAS

NOTE: COUNTER SET TO 100;
REFRESH INTERVAL 15.6 US AT 10 MHZ



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DEFINE FIRST

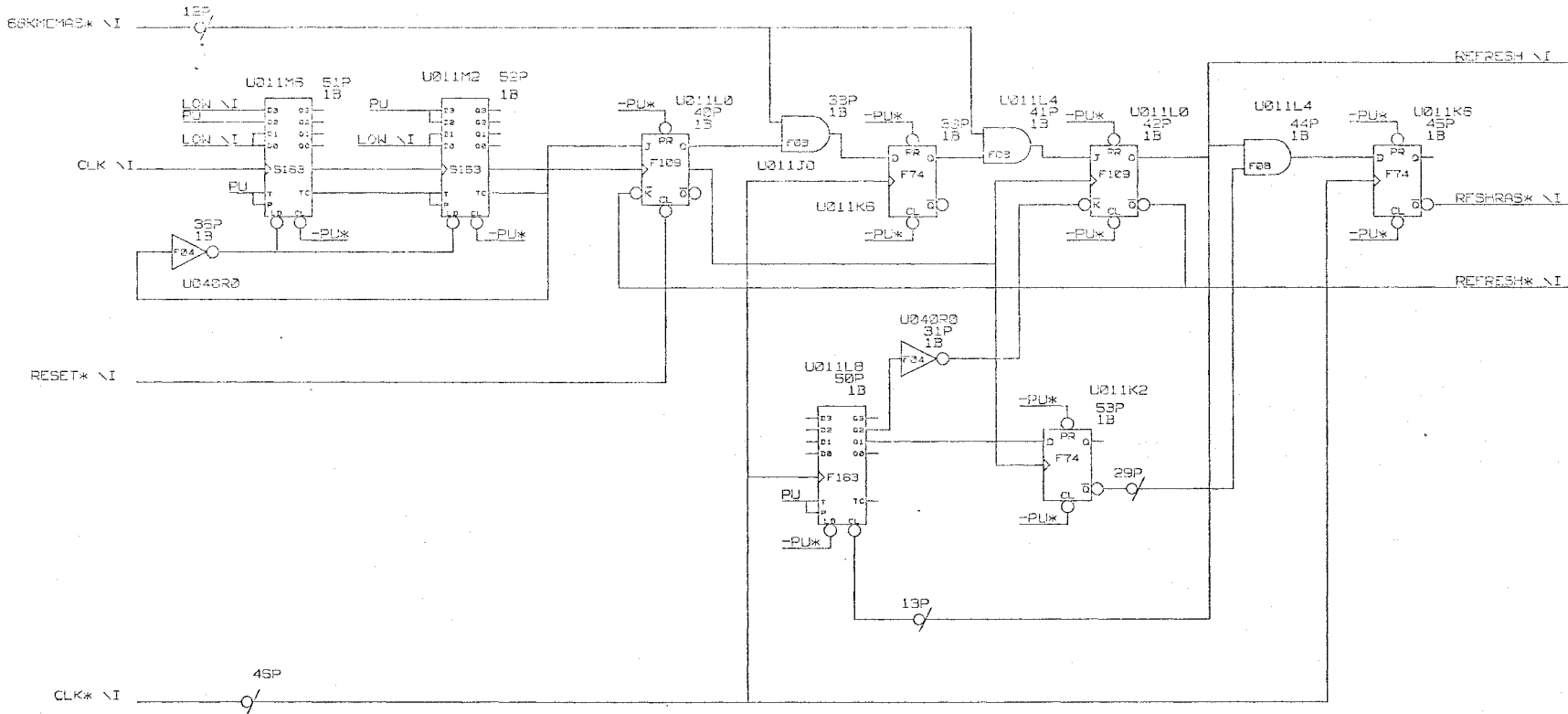


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TITLE: REFRESH CONTROL	ABBR: RFC
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Mon Sep 10 16:45:57 1984	PAGE: SPU.2 CPU.4 RFC.1

RED SYNC GRNT (RFSH) RAS

NOTE: COUNTER SET TO 100;
REFRESH INTERVAL 15.6 US AT 10 MHZ



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DEFINE
X-STEP:111

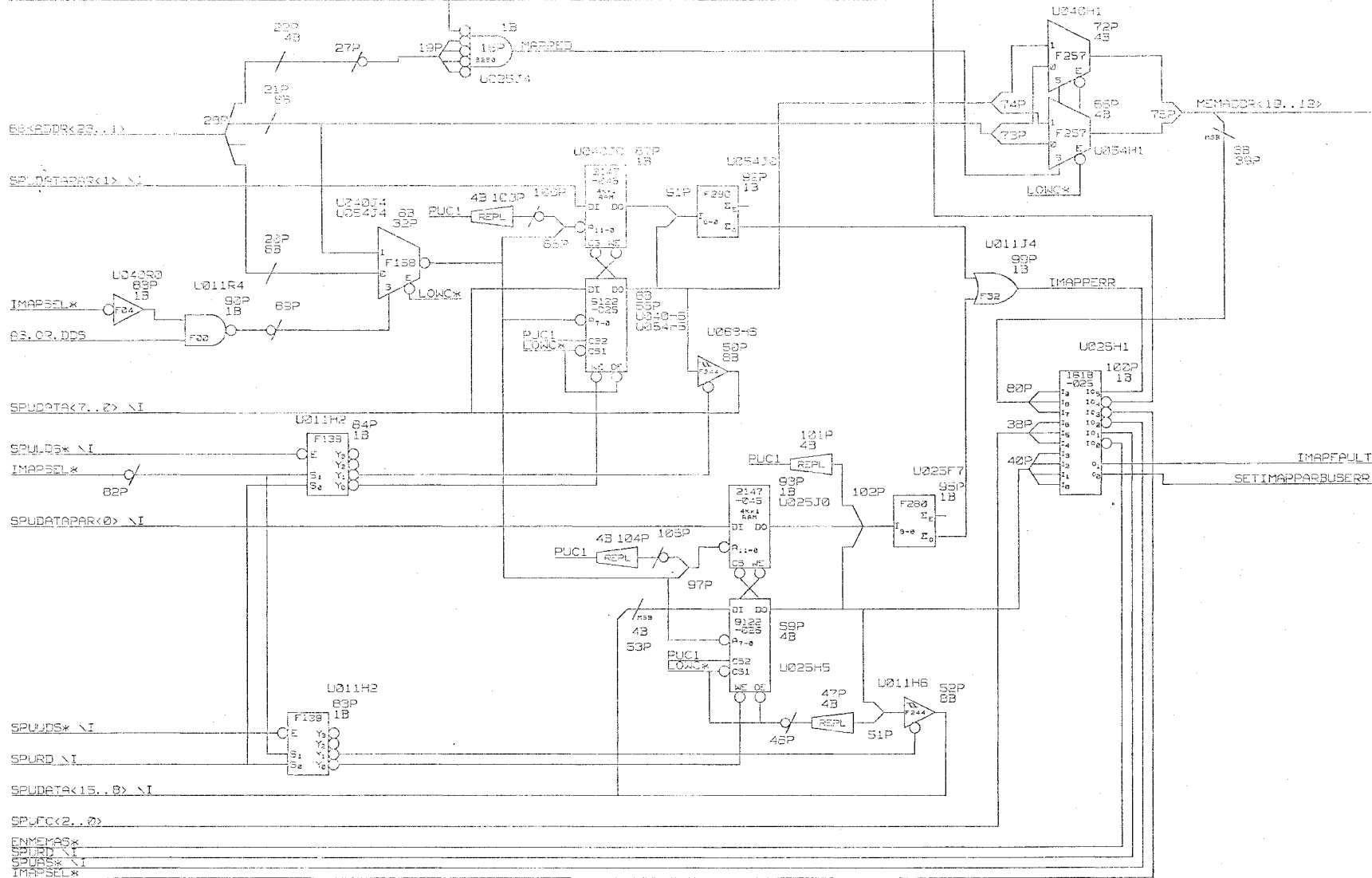


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TITLE: REFRESH CONTROL
DRAWING: 410-000131-300 D08
REVISED: Thu Jan 3 09:29:30 1985

ABBR: RFC
ENGR: NOBLES
PAGE: SPU.2 CPU.4 RFC.1

MODEL:CPU



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CONVEX

TITLE: CPU (MEMORY MAPPER)

DRAWING: 410-000131-300 D08

ABBR: CPU

ENGR: NOBLES

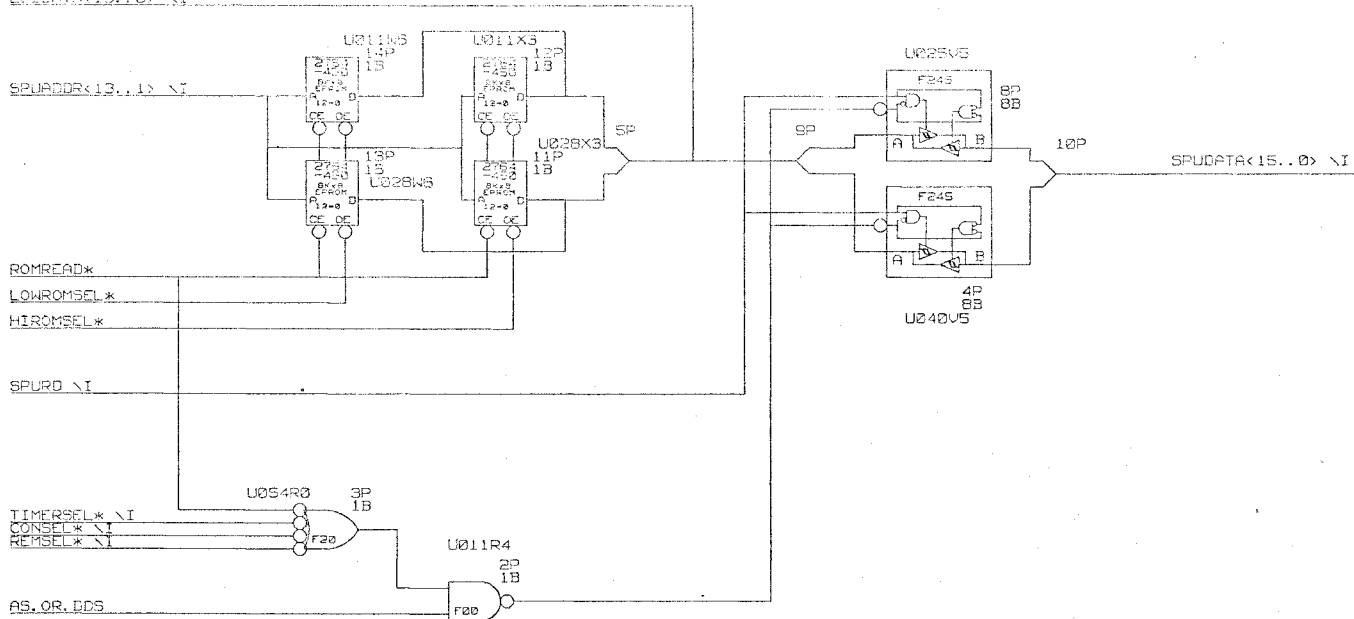
REVISED: Fri Jan 4 11:10:08 1985

PAGE:

SPU.2 CPU.5

(FROM 8251'S AND 8513)

LSIDATA<15..0> NI



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CONVEX

TITLE: CPU (ROMS & LSI DATA BUFFER)

DRAWING: 410-000131-300 D01

ABBR: CPU

ENGR: NOBLES

REVISED: Mon Sep 10 16:35:11 1984

PAGE:

SPU.2 CPU.7

8

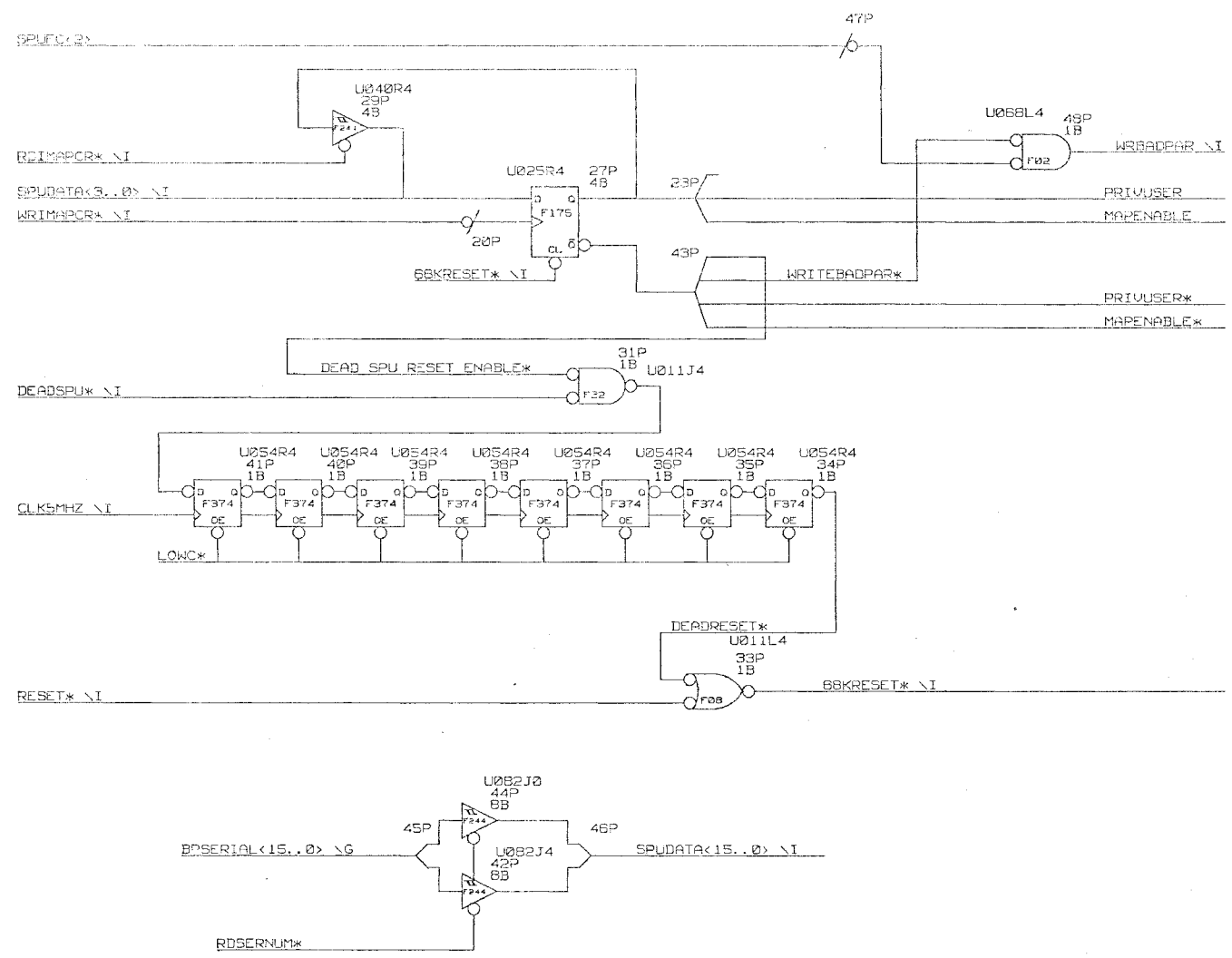
7

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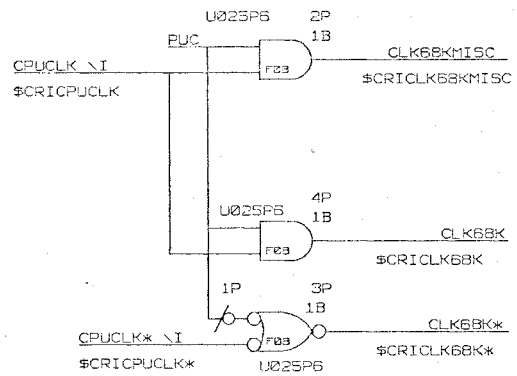
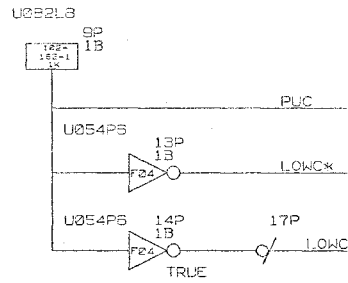
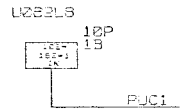
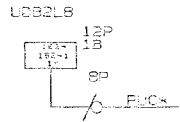


TITLE: CPU (MISC REGS)
DRAWING: 410-000131-300 D01

ABBR: CPU
ENGR: NOBLES

REVISED: Tue Sep 11 11:06:39 1984

PAGE: SPU.2 CPU.8



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CONVEX

TITLE: CPU (PULLUPS AND CLOCKS)

ABBR: CPU

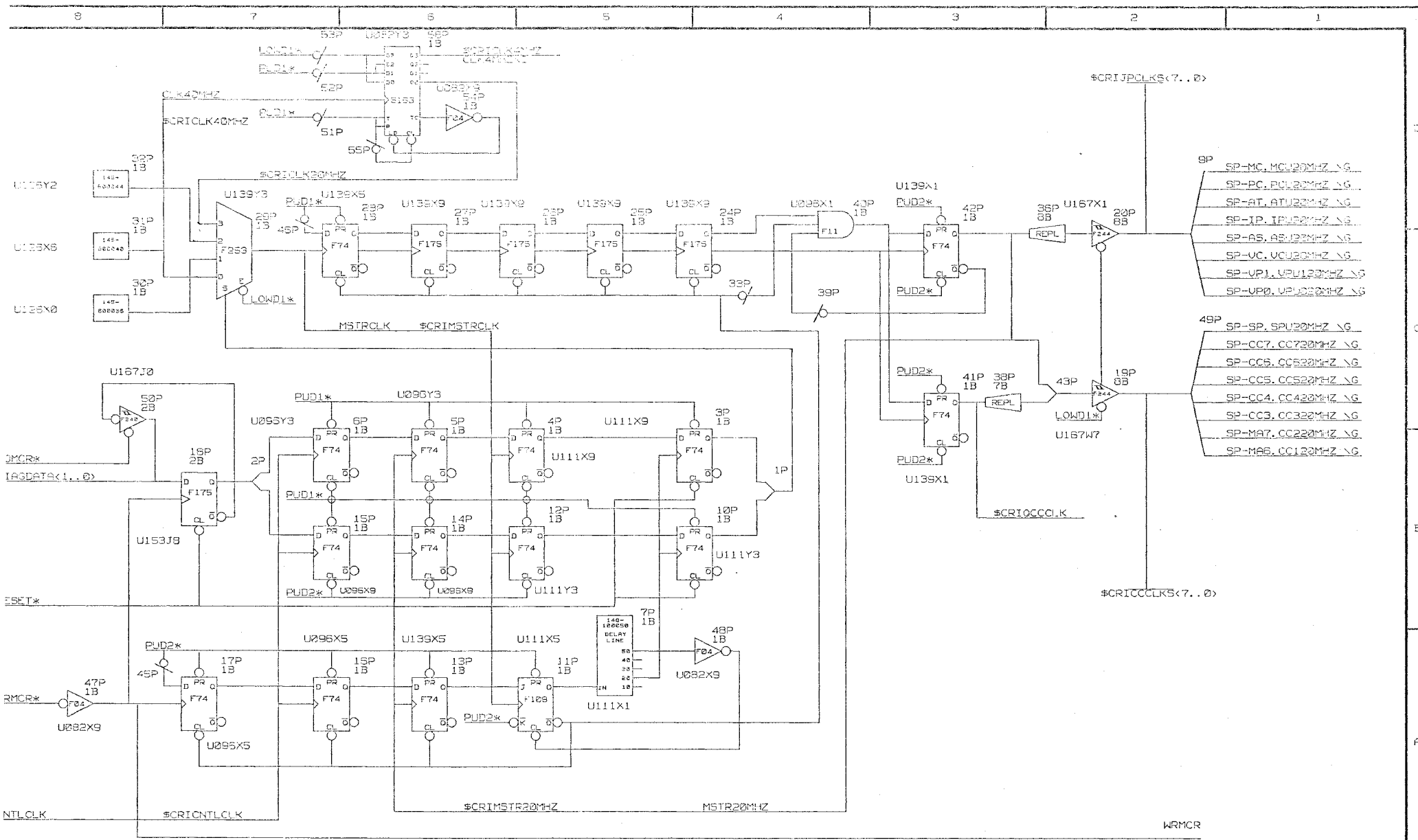
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ENGR: NOBLES

REVISED: Mon Jan 7 17:04:48 1985

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SPU, 2 CPU, 9



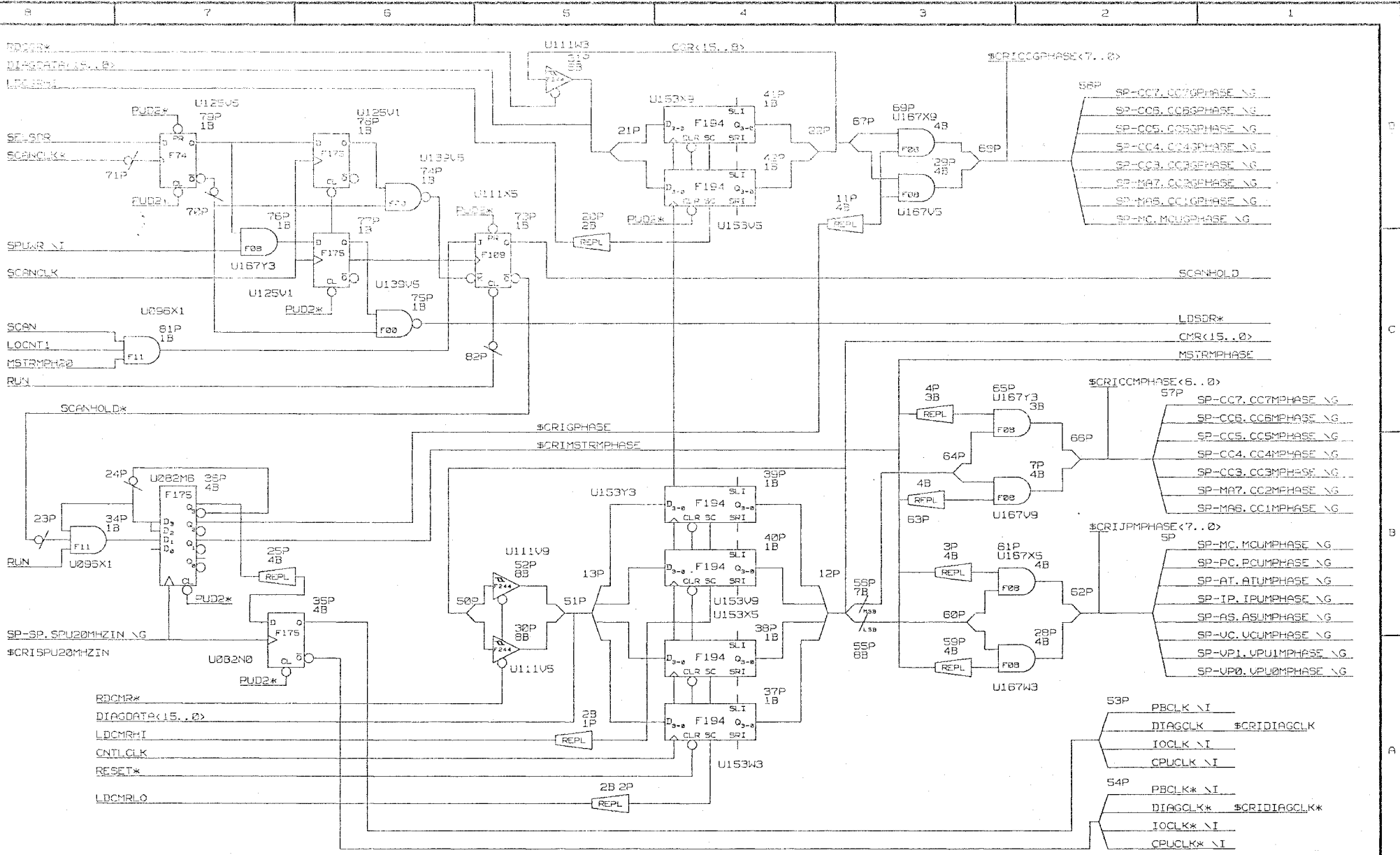
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REFINE
X-FIRST
X-STEP



CONVEX

TITLE: DIAG	ABBR: DIAG
DRAWING: 410-000131-300 D08	ENGR: NOBLES
REVISED: Thu Jan 3 14:27:01 1985	PAGE: SPU.2 DIAG.1
3	2
	1



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CONVEX

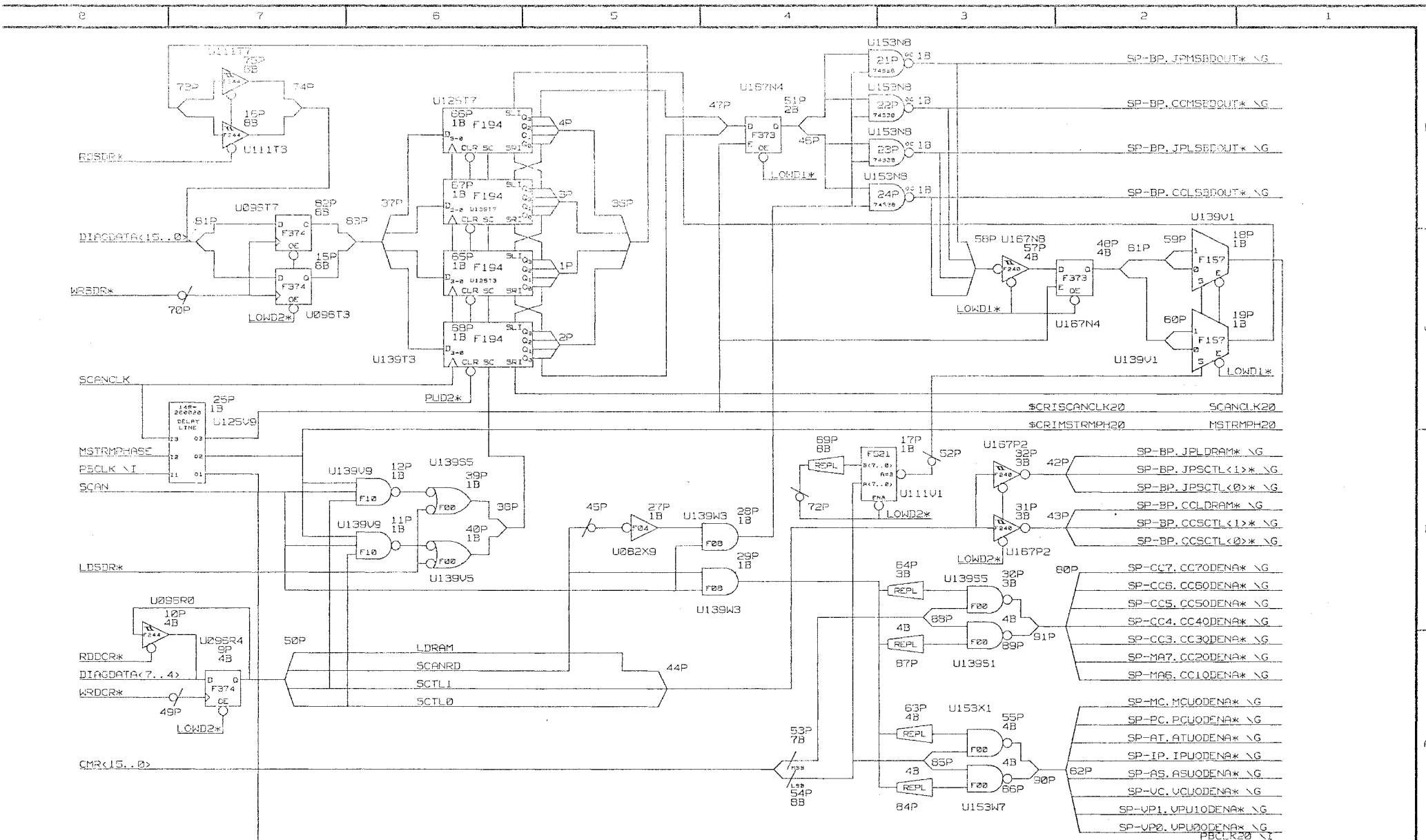
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DRAWING: 410-000131-300 D01

ABBR: DIAG
ENGR: NOBLES

REVISED: Fri Sep 14 11:02:35 1984

PAGE:

SPU.2 DIAG.2



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CONVEX

TITLE: DIAG (SCAN INTERFACE)

ABBR: DIAG

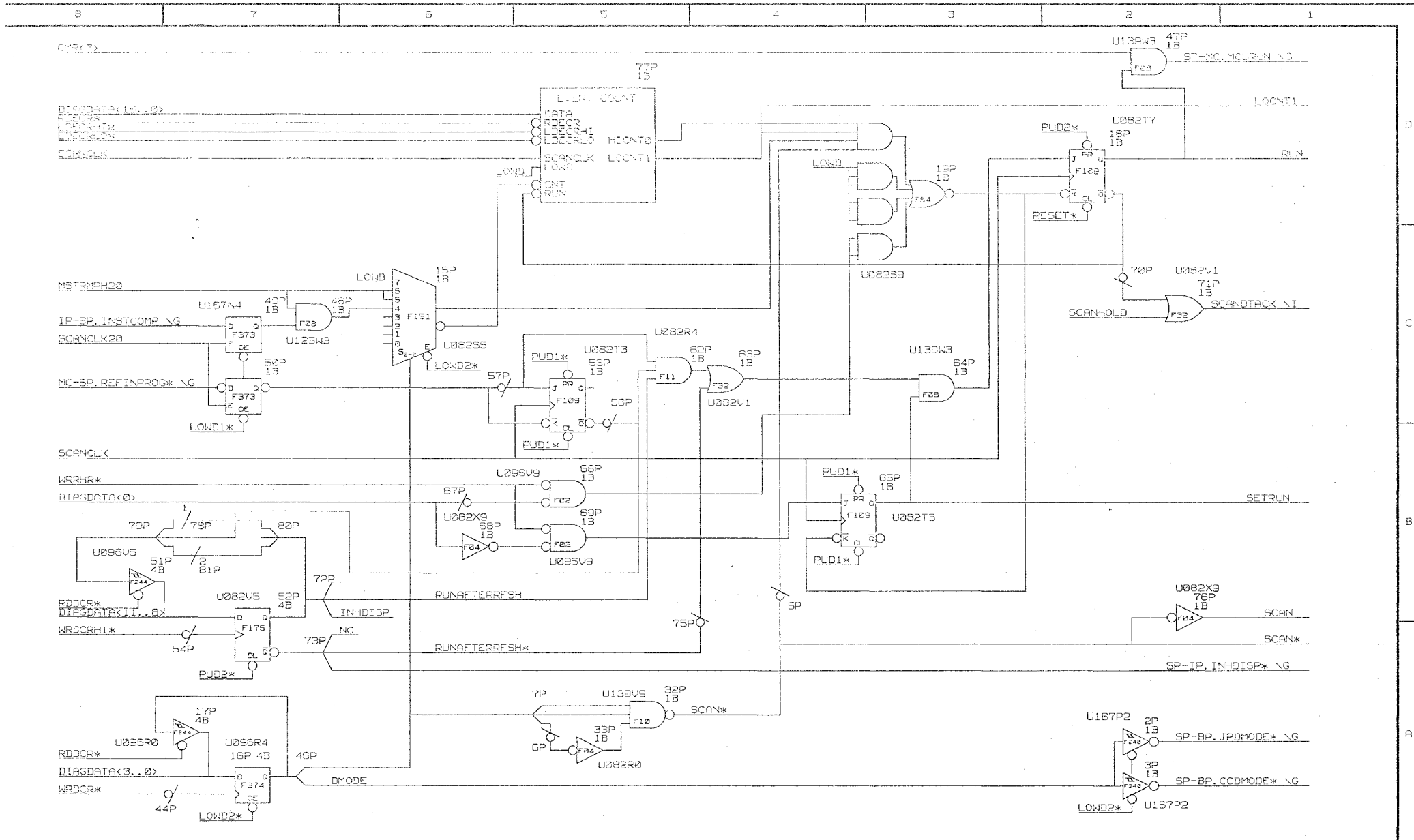
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ENGR: NOBLES

REVISED: Fri Sep 14 11:04:03 1984

PAGE:

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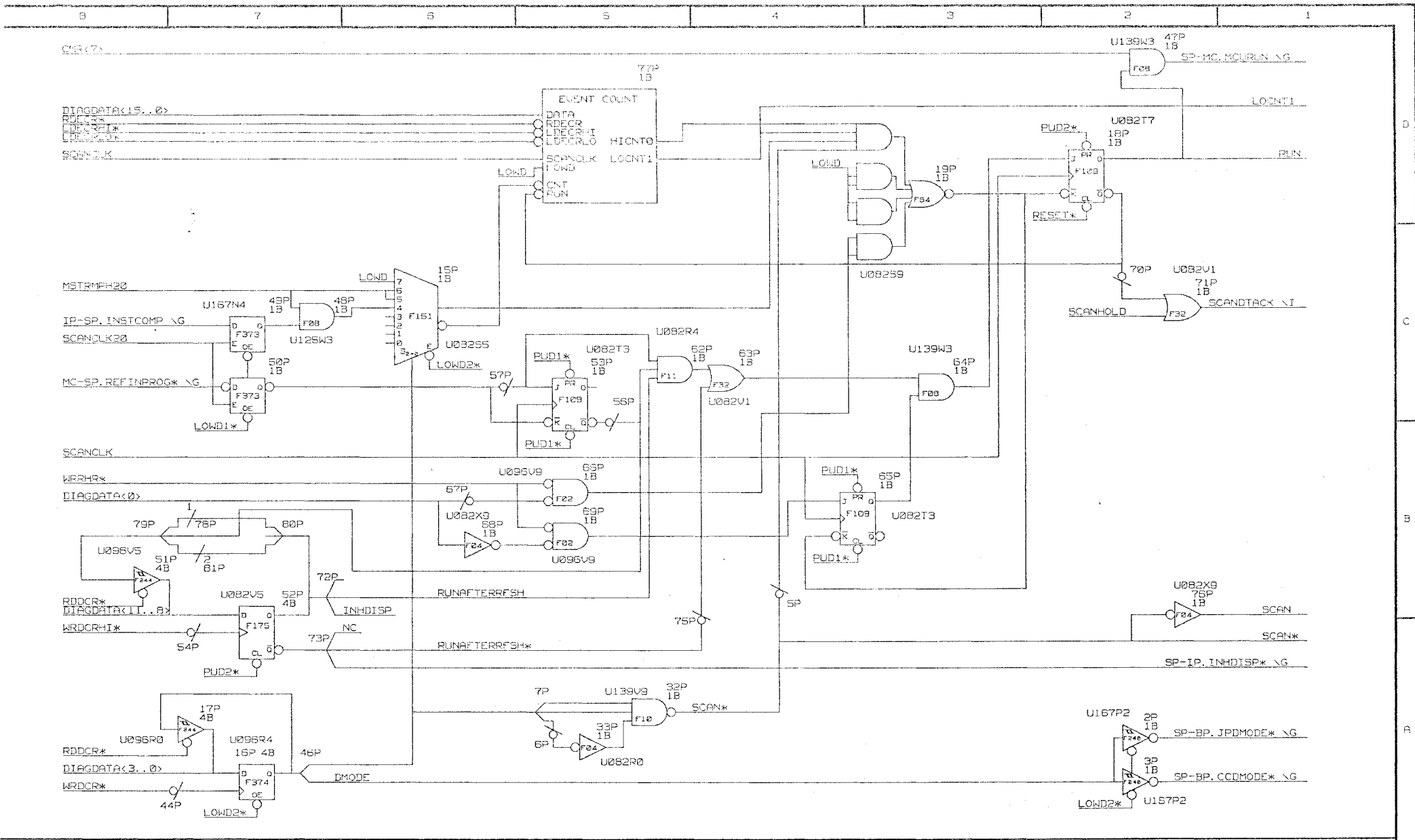


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CONVEX

TITLE: DIAG (RUN CONTROL)		ABBR: DIAG
DRAWING: 410-002131-300 D03		ENGR: NOBLE5
REVISED: Thu Jan 3 17:13:51 1985	PAGE:	SPU.2 DIAG.4



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CONVEX

TITLE: DIAG (RUN CONTROL)

DRAWING: 410-000131-300 D01

REVISED: Fri Sep 14 11:05:29 1984

ABBR: DIAG

ENGR: NOBLES

PAGE: SPU.2 DIAG.4

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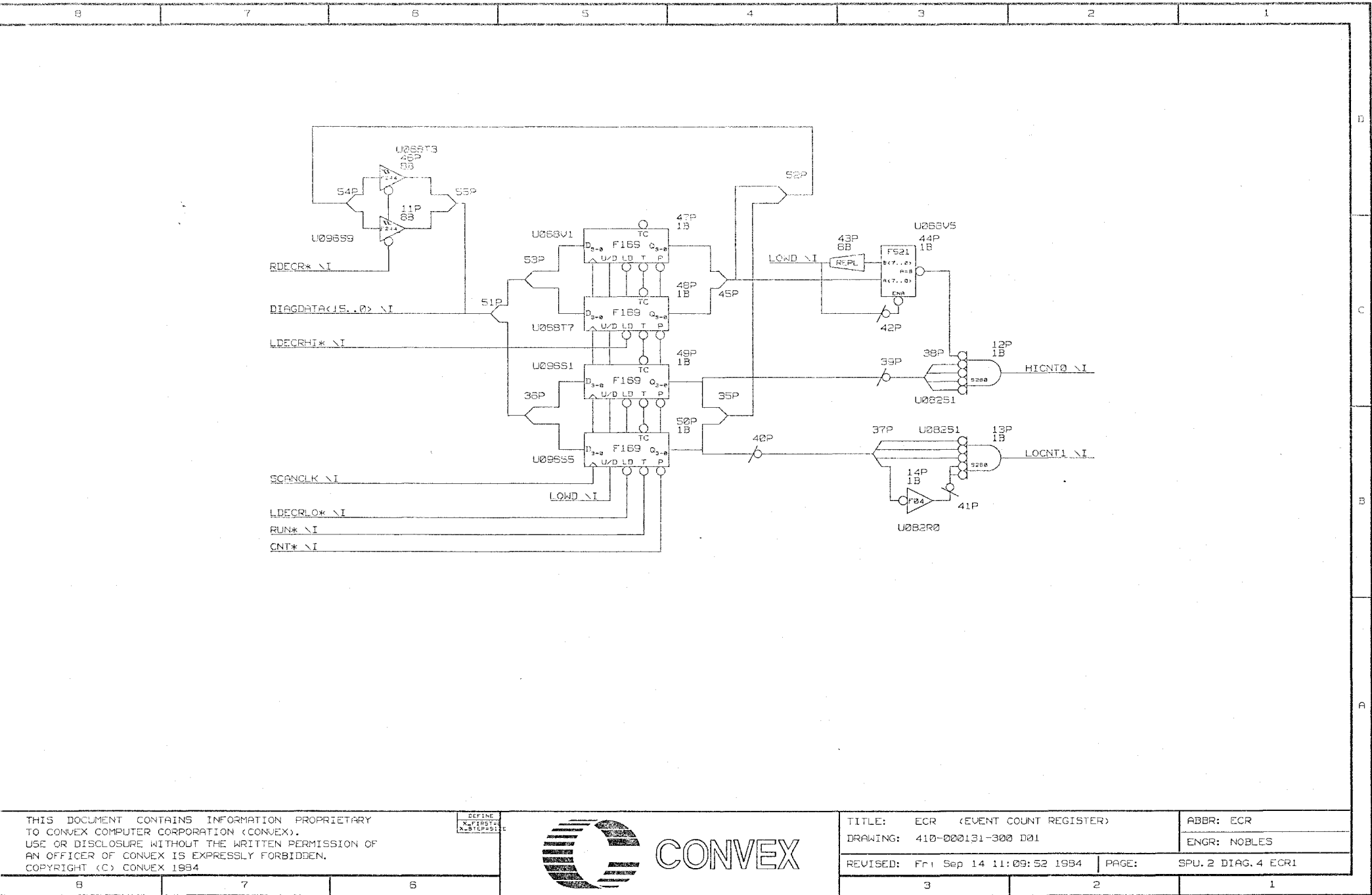
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1



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DEFINE
X-FIRST
Q-STOP



CONVEX

TITLE: ECR (EVENT COUNT REGISTER)

ABBR: ECR

DRAWING: 410-000131-300 D01

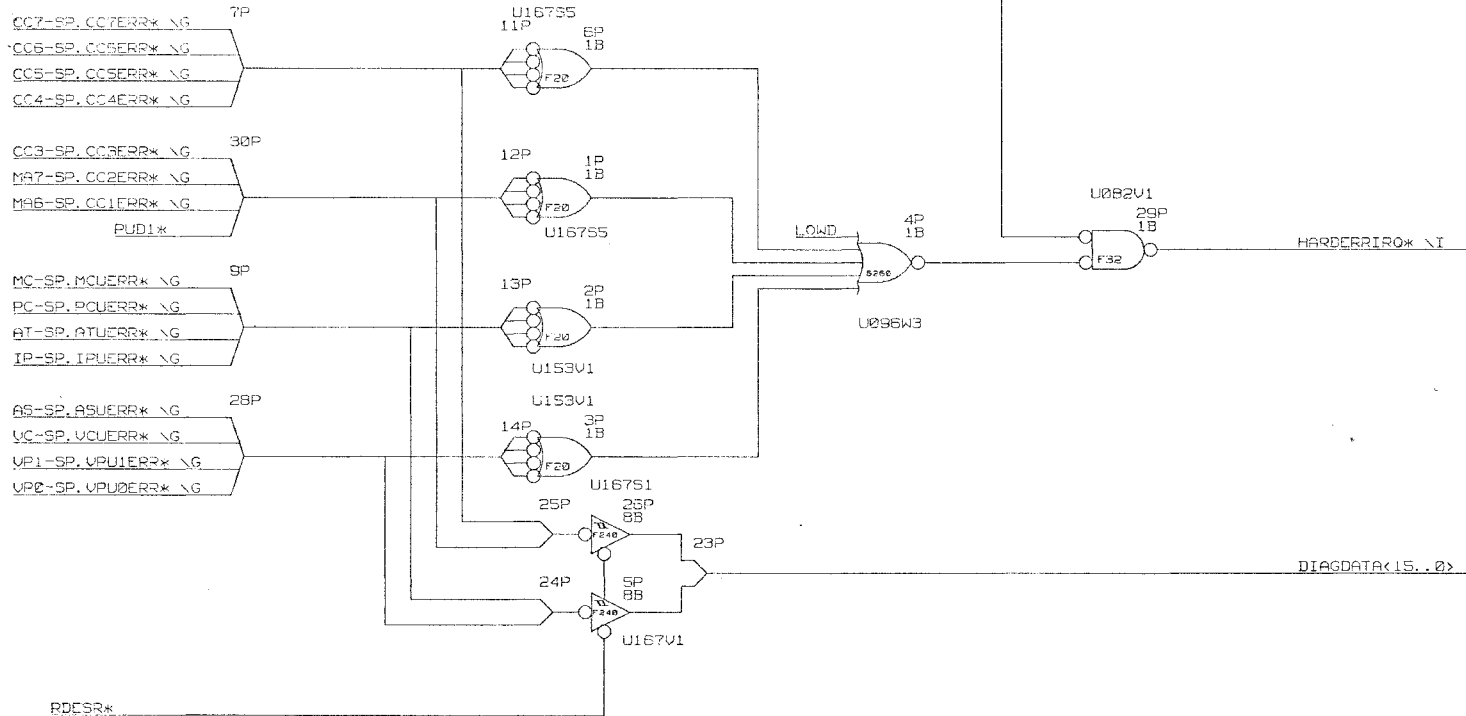
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REVISED: Fri Sep 14 11:09:52 1984

PAGE:

SPU.2 DIAG.4 ECR1

-SOANK



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CONVEX

TITLE: DIAG (ERROR SOURCE REGISTER)

ABBR: DIAG

DRAWING: 410-000131-300 D01

ENGR: NOBLES

REVISED: Fri Sep 14 11:06:03 1984

PAGE:

SPU.2 DIAG.5

B

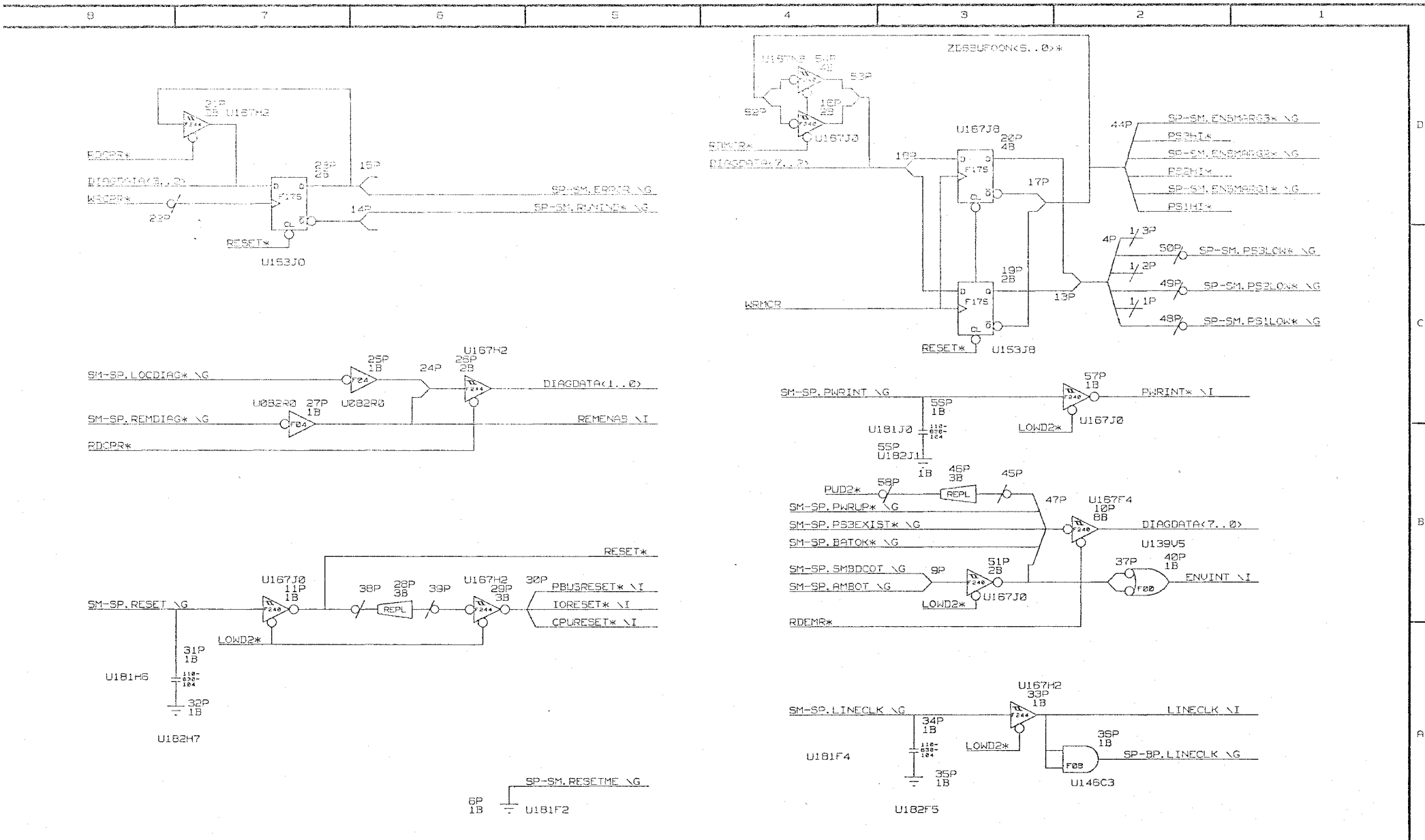
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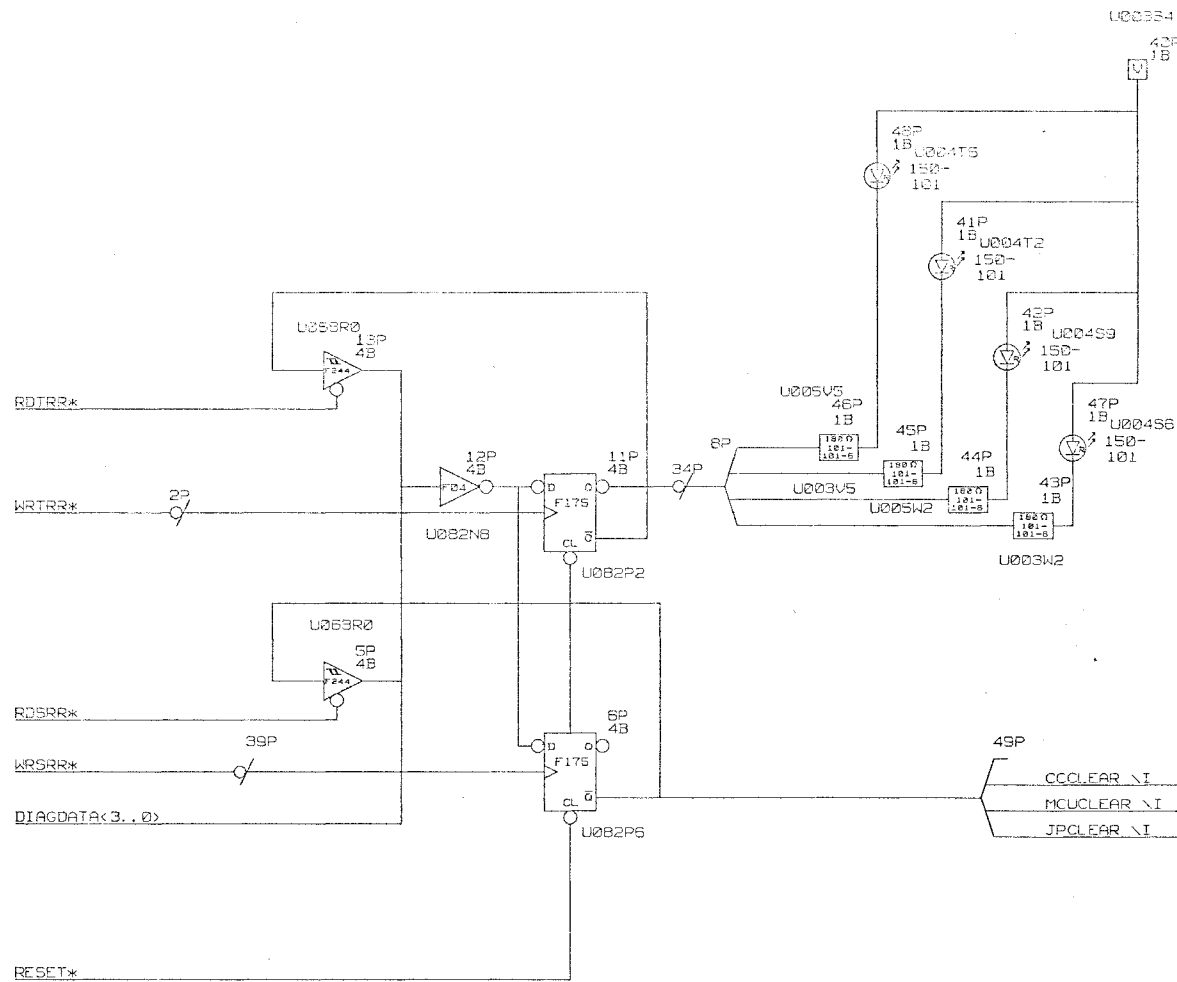


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CONVEX

TITLE: DIAG (SMB INTERFACE)		ABBR: DIAG
DRAWING: 410-000131-300 D01		ENGR: NOBLES
REVISED: Fri Sep 14 11:06:53 1984	PAGE:	SPU.2 DIAG.6



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TITLE: DIAG (SRR AND TRR)

DRAWING: 410-000131-300 D01

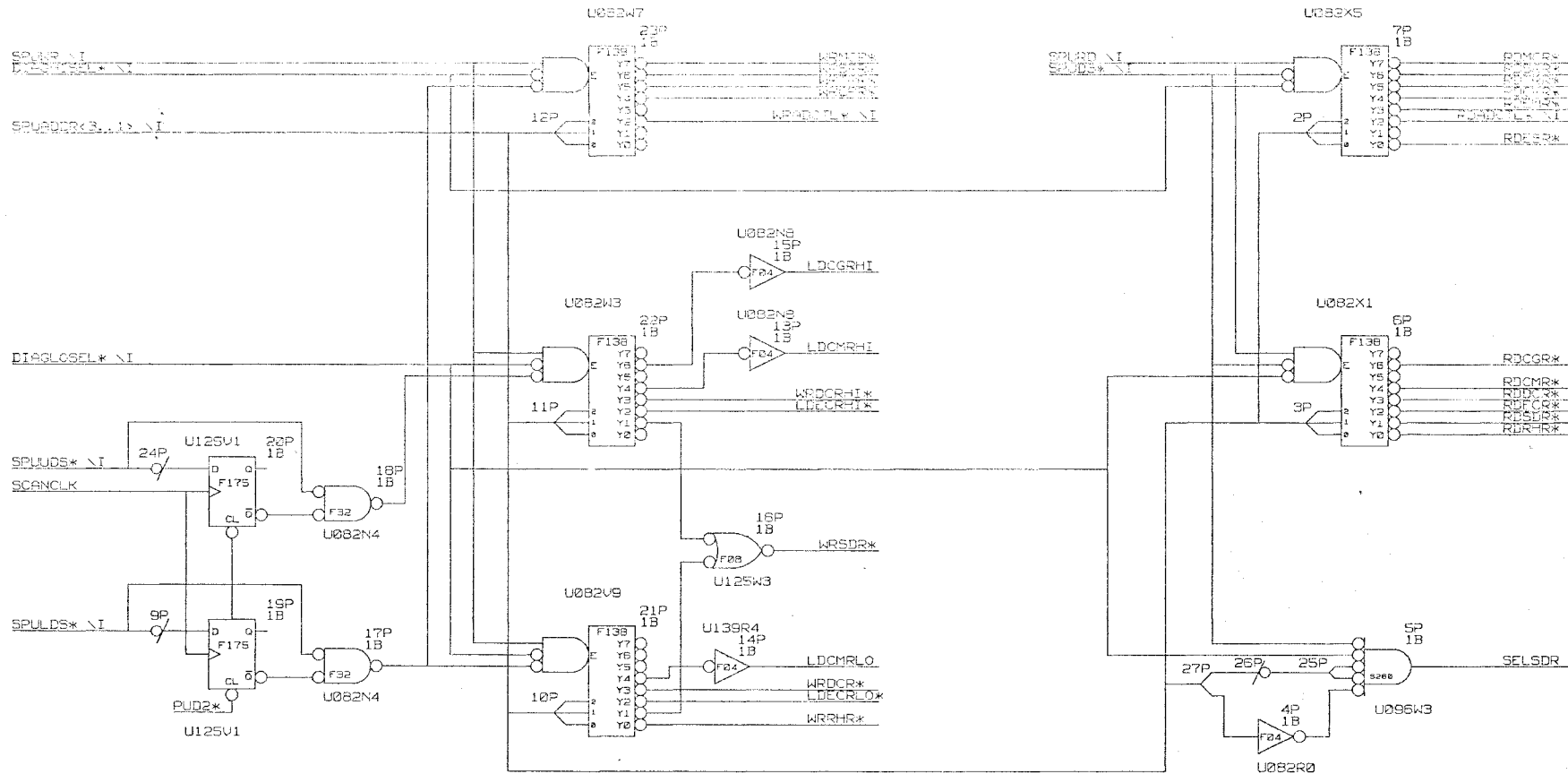
REVISED: Fri Sep 14 11:07:38 1984

PAGE:

ABBR: DIAG

ENGR: NOBLES

SPU.2 DIAG.7



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TITLE: DIAG (REGISTER SELECTS)

ABBR: DIAG

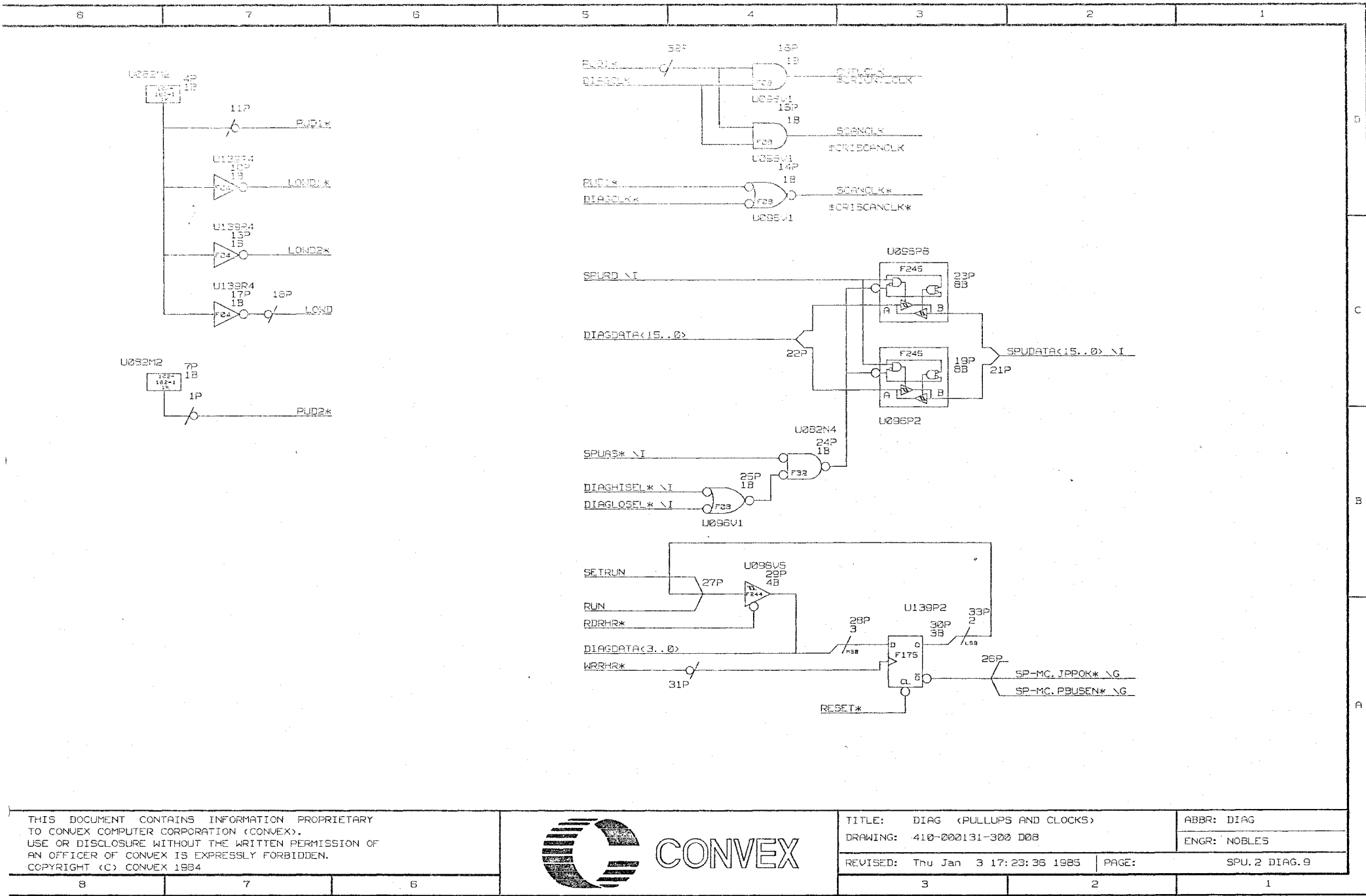
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ENGR: NOBLES

REVISED: Fri Sep 14 11:08:21 1984

PAGE:

SPU.2 DIAG.8

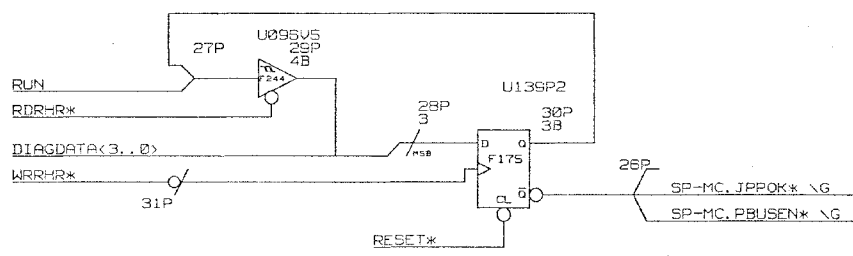
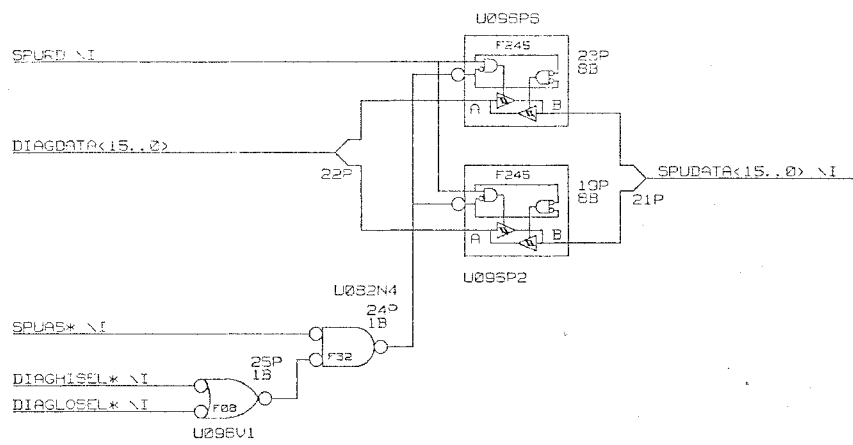
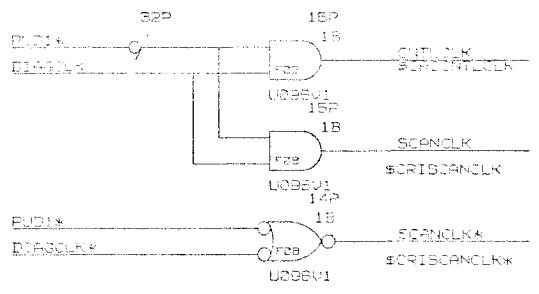
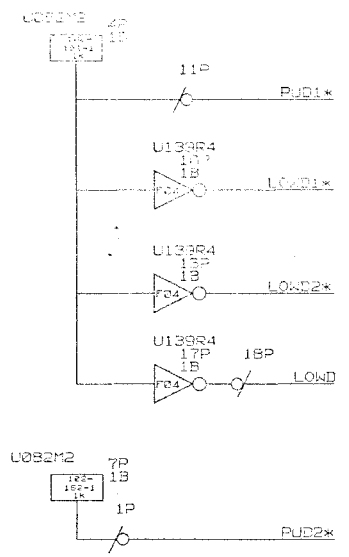


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TITLE: DIAG (PULLUPS AND CLOCKS)
 DRAWING: 410-000131-300 D08
 REVISED: Thu Jan 3 17:23:36 1985

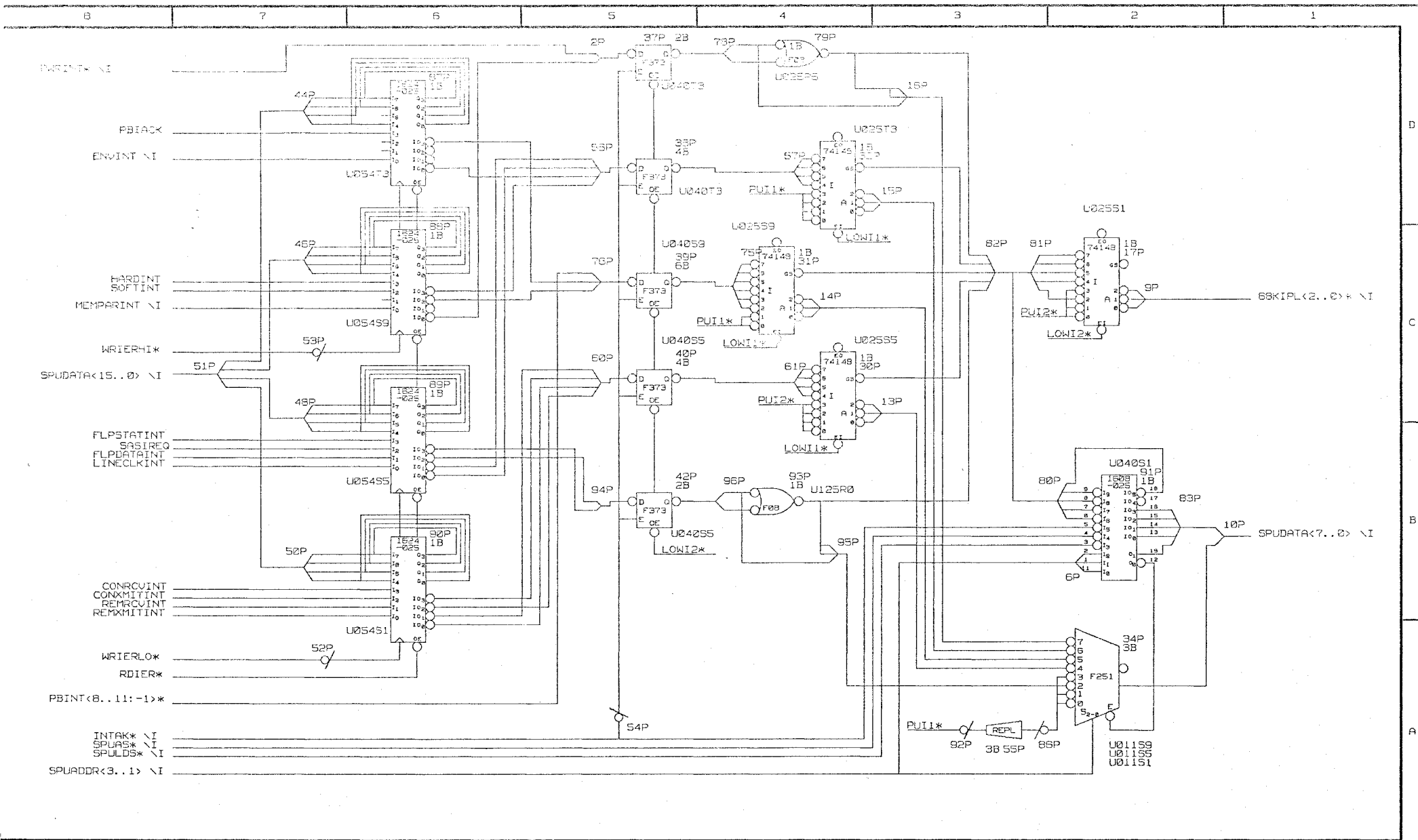
ABBR: DIAG
 ENGR: NOBLES
 PAGE: SPU.2 DIAG.9



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TITLE: DIAG (PULLUPS AND CLOCKS)	ABBR: DIAG
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Fri Sep 14 11:09:01 1984	PAGE: SPU.2 DIAG.9

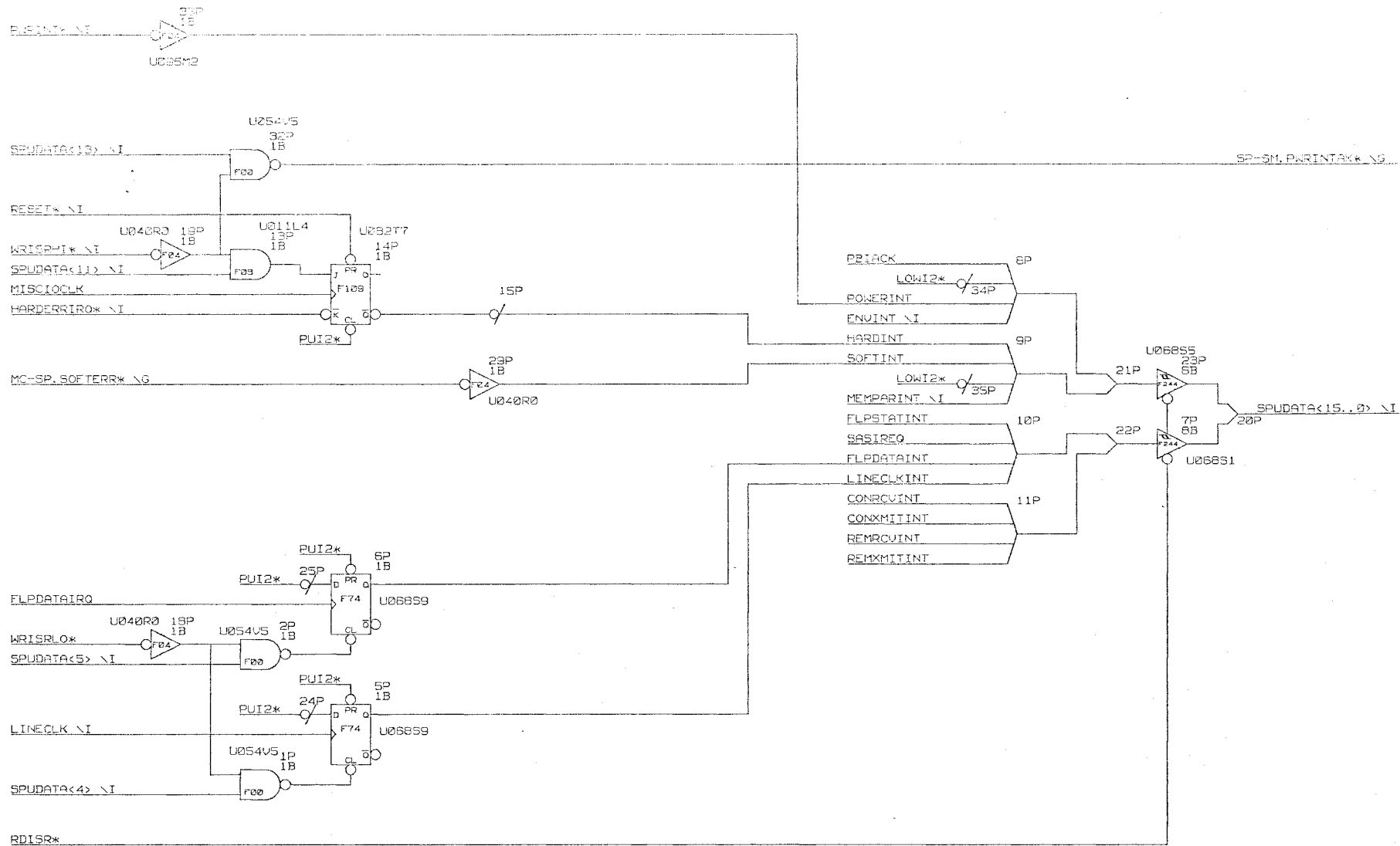


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DEFINITIONS
X-FIRST STEP
X-STEP#2



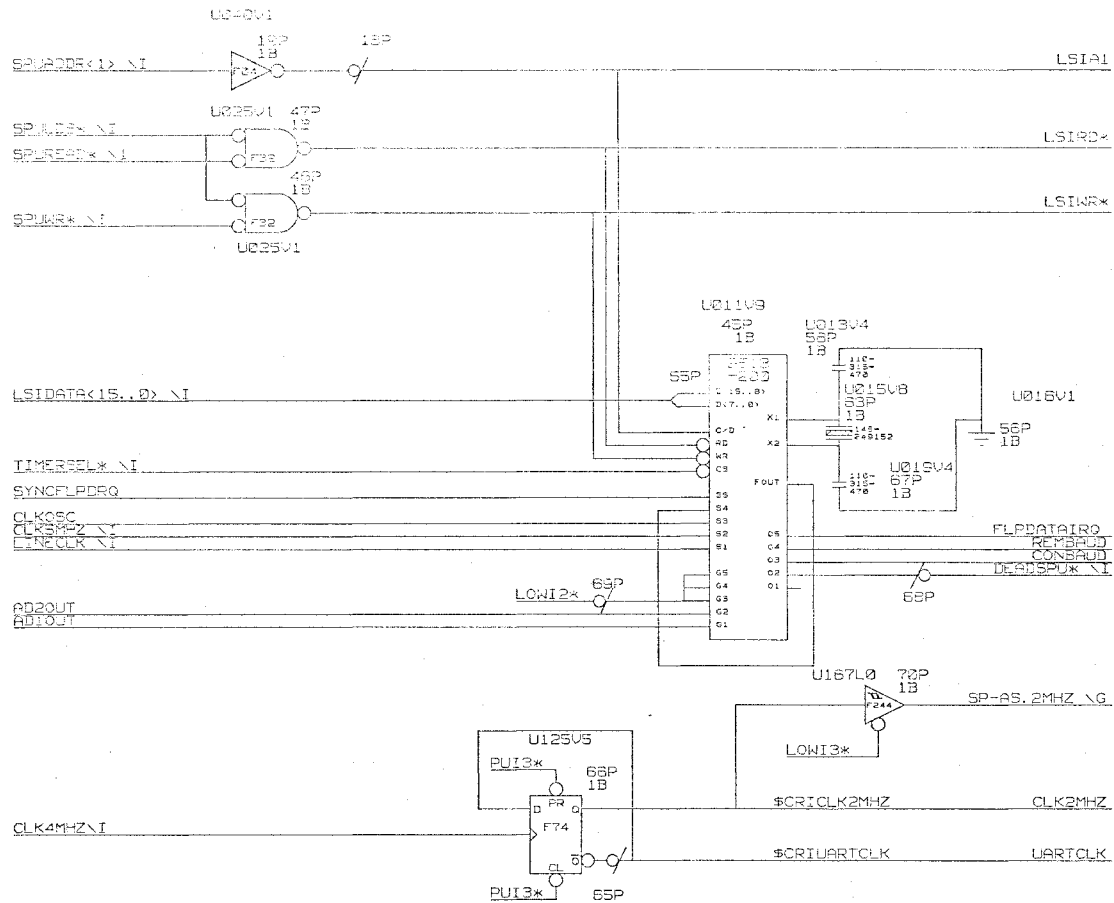
TITLE: IO (INTERRUPT CONTROLLER)
 DRAWING: 410-000131-300 D01
 REVISED: Mon Sep 10 16:48:36 1984
 ASBR: IO
 ENGR: NOBLES
 PAGE: SPU.2 IO.1



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TITLE: IO (INTERRUPT STATUS REG)	ABBR: IO
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Mon Sep 10 16:49:23 1984	PAGE: SPU.2 IO.2



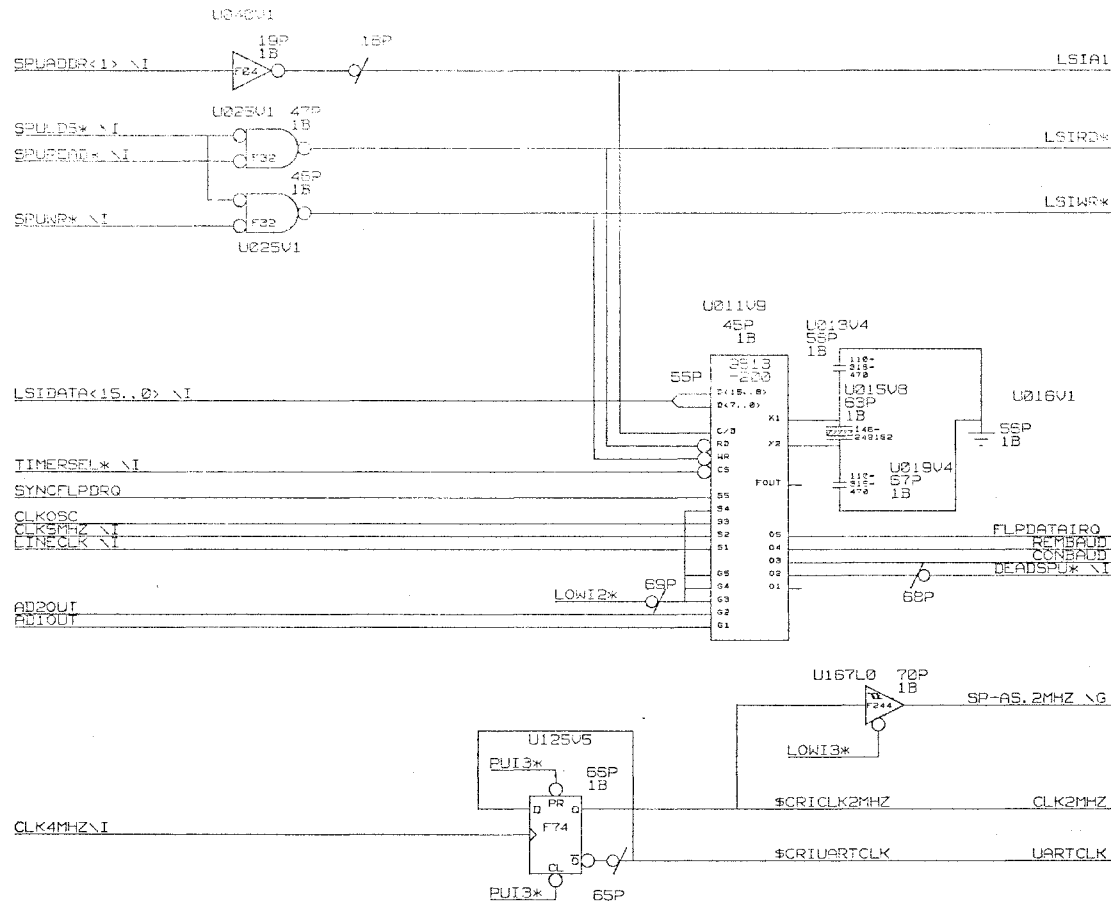
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TITLE: IO (TIMER)
DRAWING: 412-000131-300 D08

ABBR: IO
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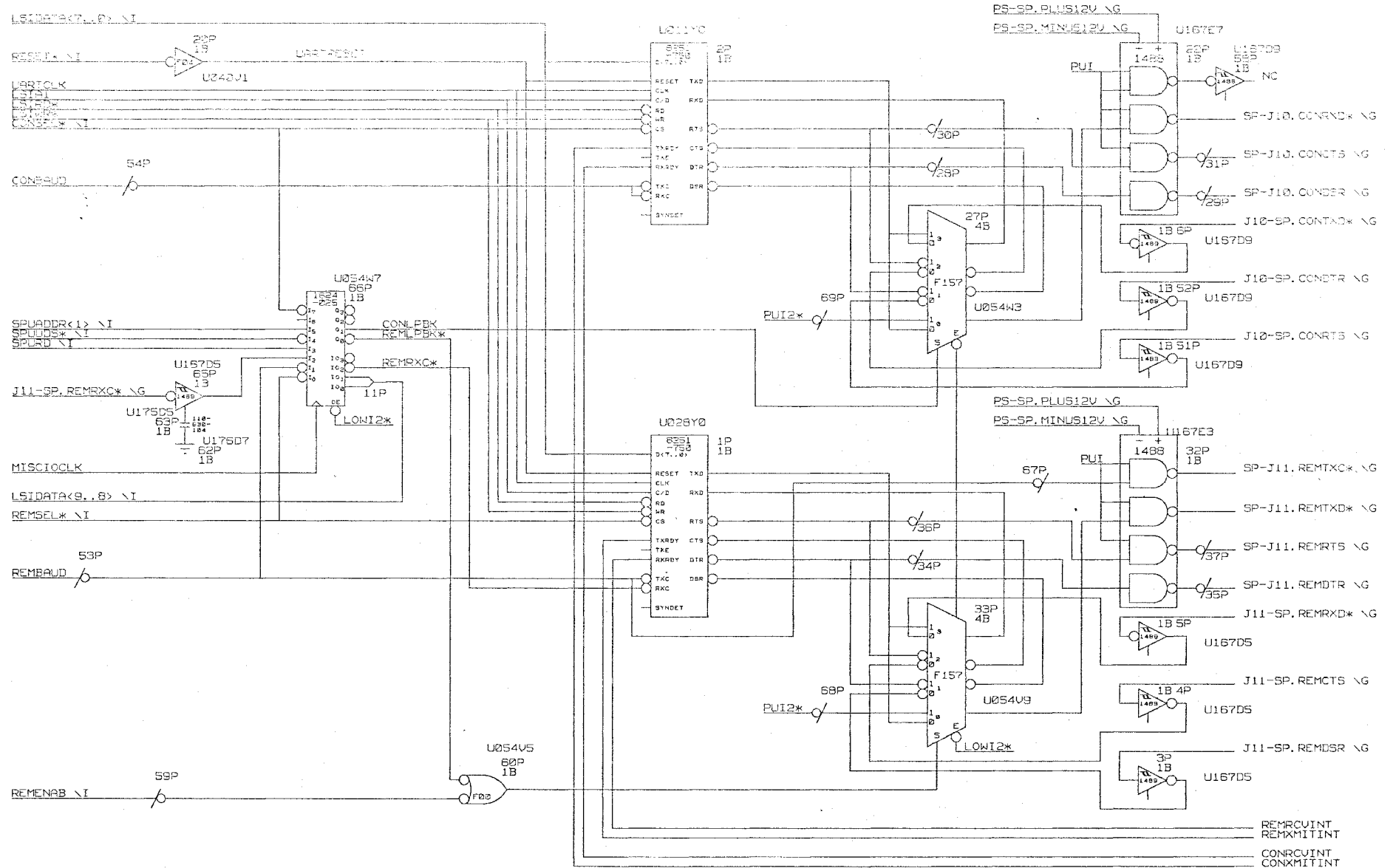
REVISED: Thu Jan 3 10:47:52 1985 PAGE: SPU.2 IO.3



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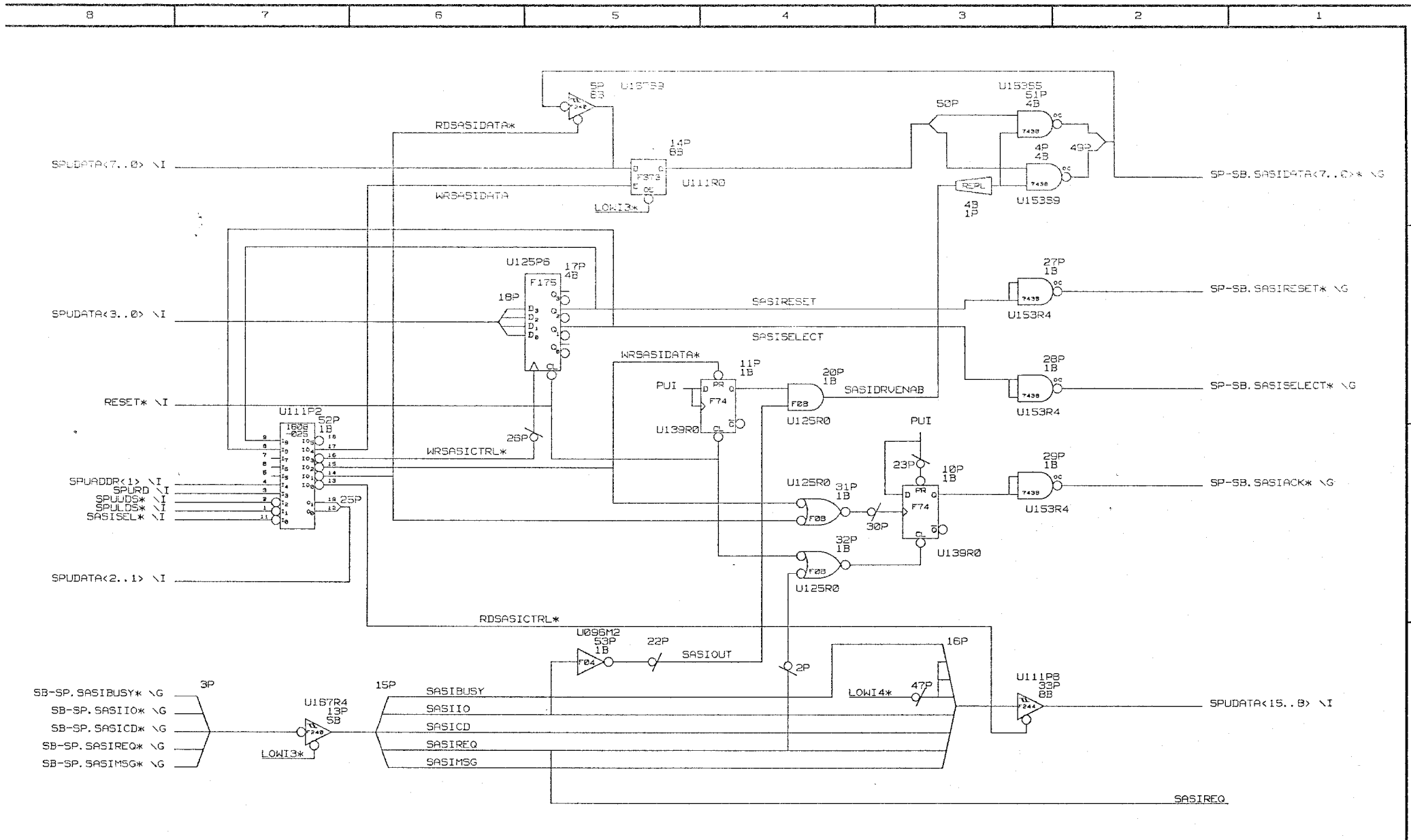
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REVISED: Tue Sep 11 11:27:36 1984	PAGE: SPU.2 IO.3



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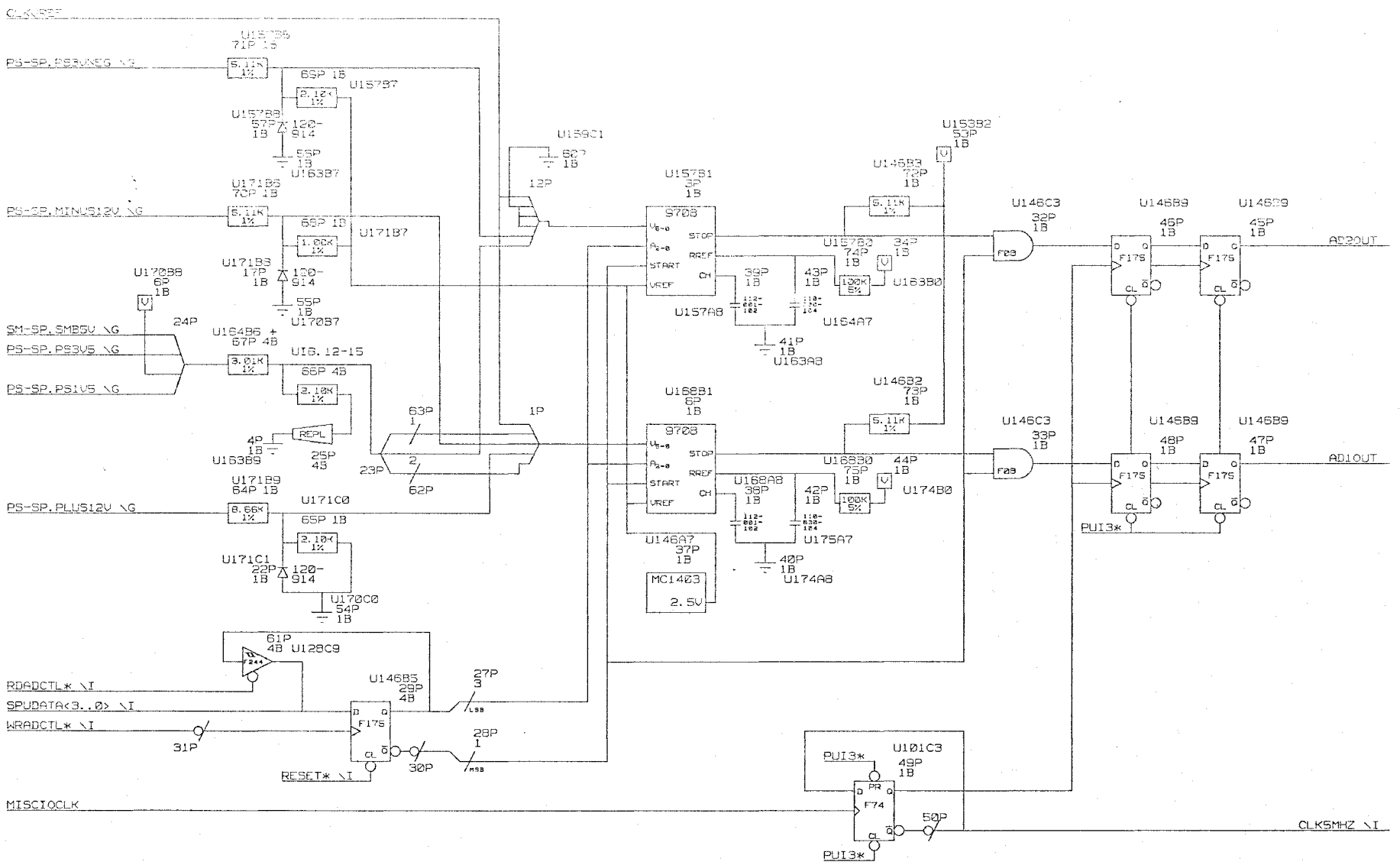
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REVISED: Mon Sep 10 16:50:55 1984	PAGE: SPU.2 I0.4



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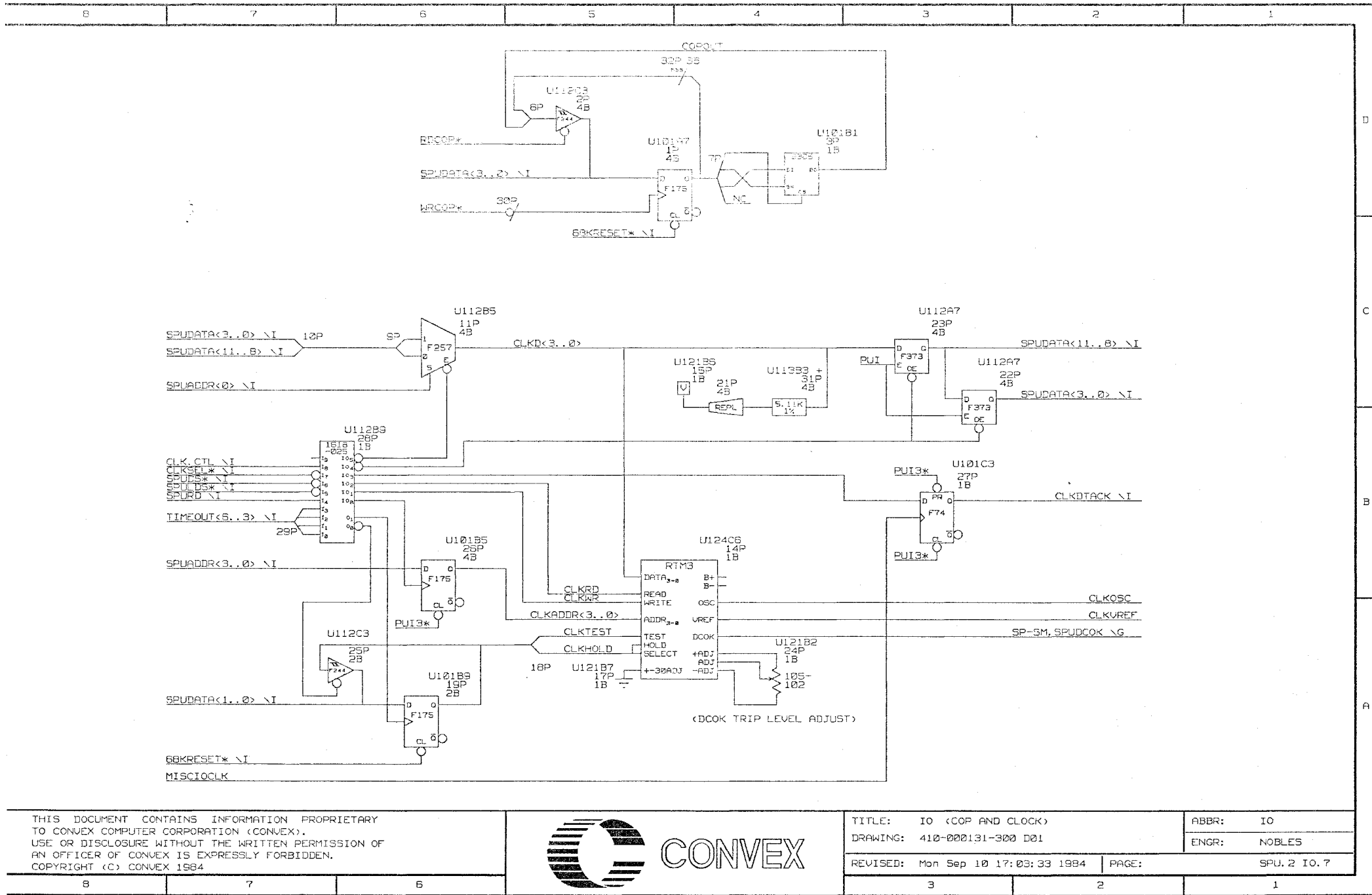
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REVISED: Mon Sep 10 16:51:42 1984	PAGE: SPU.2 IO.5



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TITLE: IO (A/D CONVERTERS)
 DRAWING: 410-000131-300 D01
 REVISID: Mon Sep 10 17:02:44 1984
 ABBR: IO
 ENGR: NOBELS
 PAGE: SPU.2 IO.6



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TITLE: IO (COP AND CLOCK)

DRAWING: 410-000131-300 D01

REVISED: Mon Sep 10 17:03:33 1984

ABBR: IO

ENGR: NOBLES

PAGE: SPU. 2 IO. 7

8

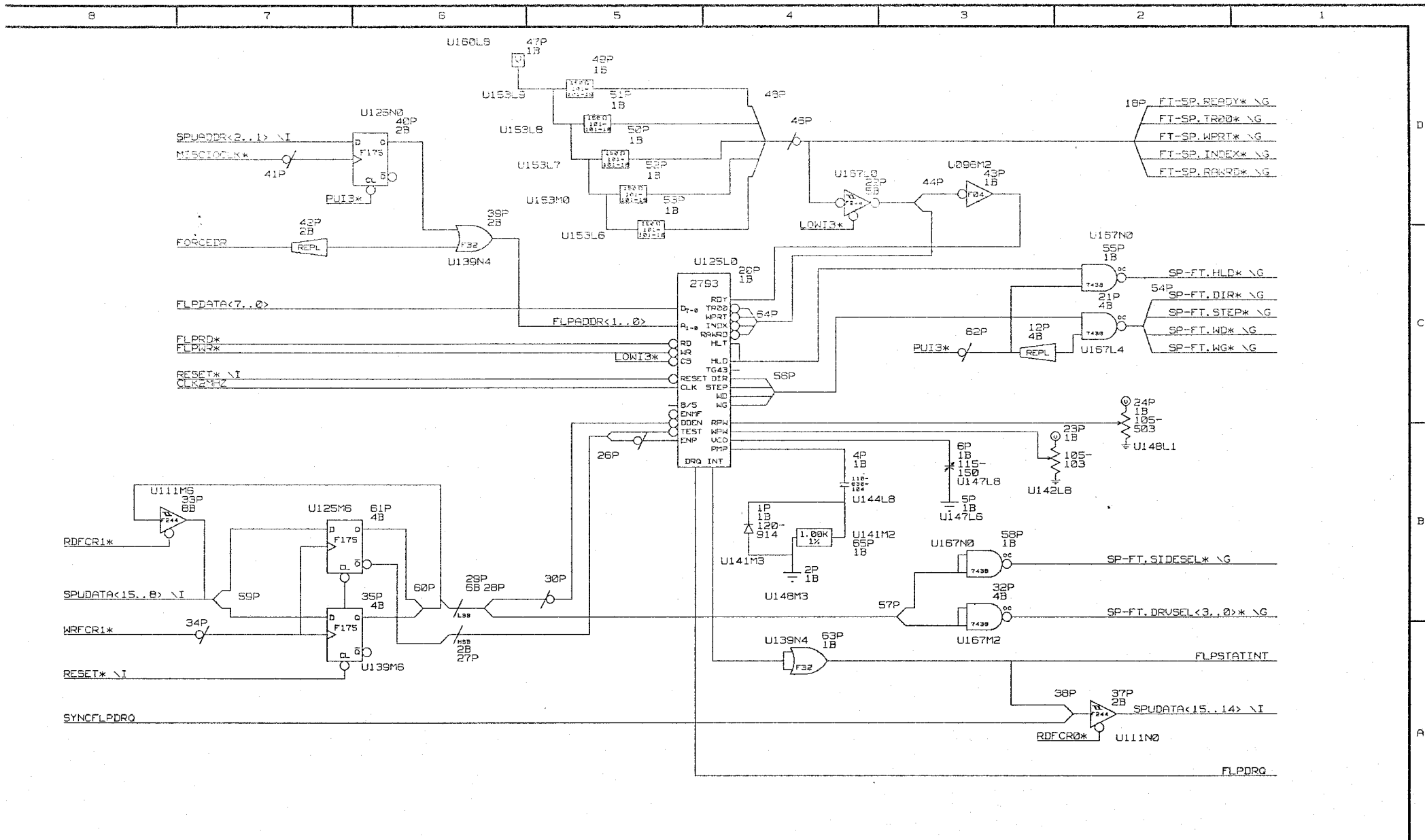
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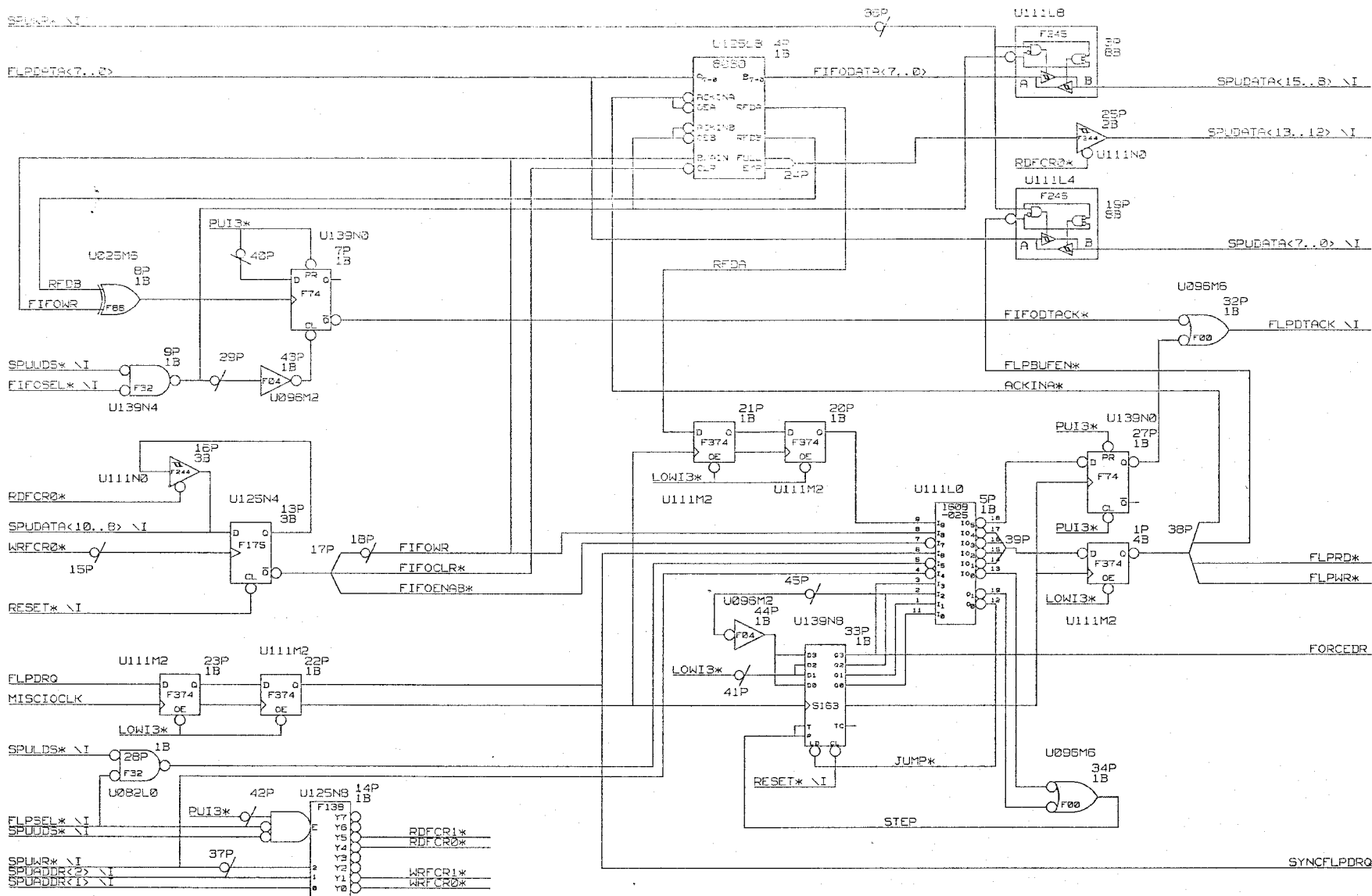
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TITLE: IO (FLOPPY INTERFACE)	ABBR: IO
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Mon Sep 10 17:11:11 1984	PAGE: SPU.2 IO.8



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CONVEX

TITLE: IO (FLOPPY CONTROL & FIFO)

DRAWING: 410-000131-300 D03

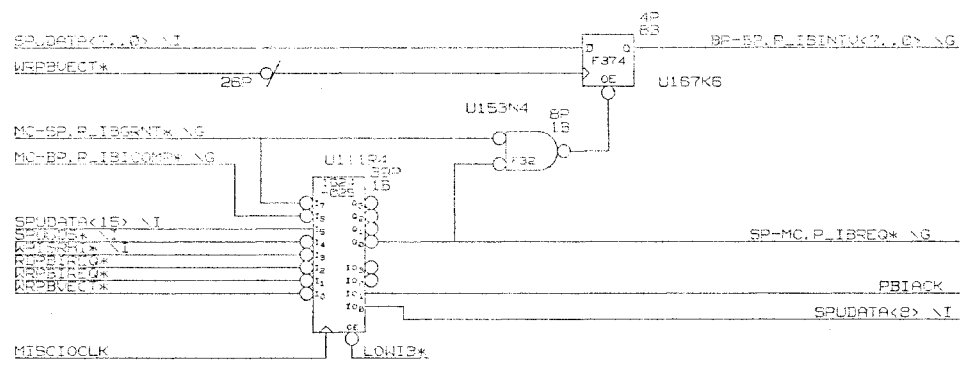
REVISED: Thu Jan 3 09:40:36 1985

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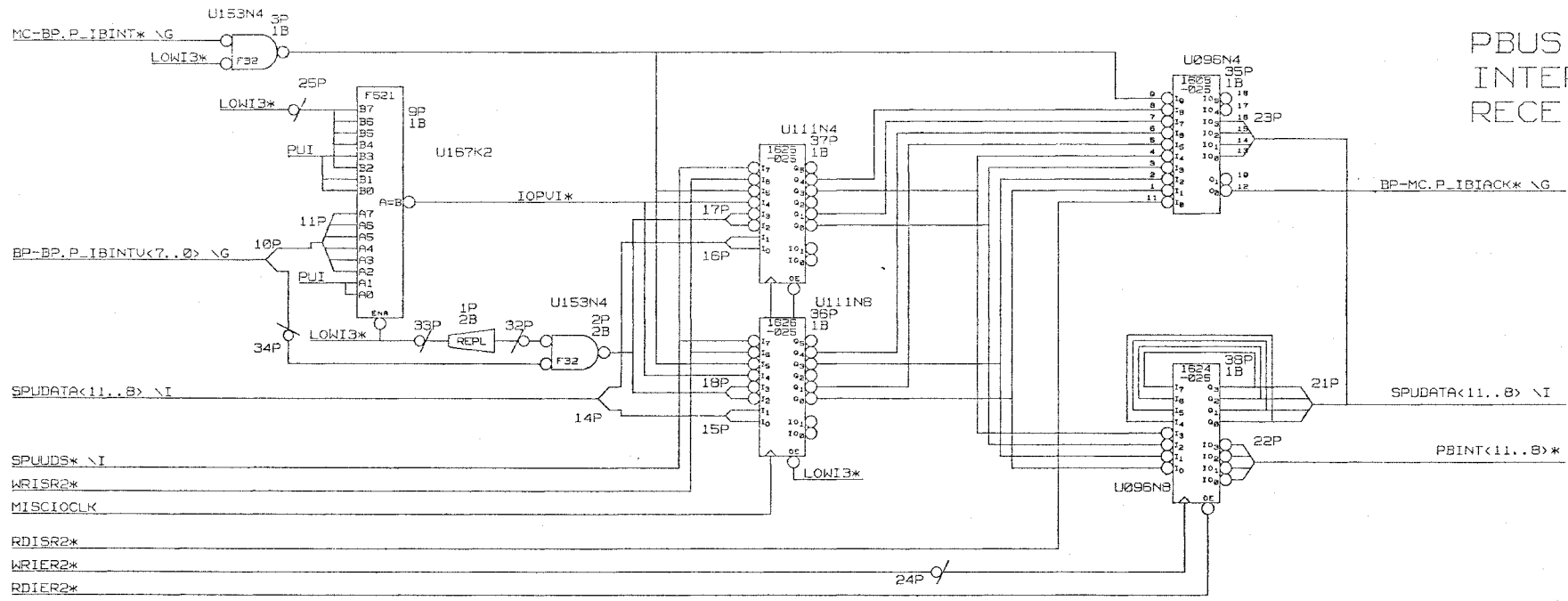
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SPU.2 IO.9



PBUS INTERRUPT TRANSMITTER

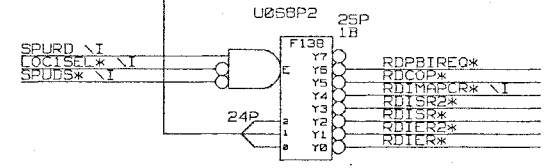
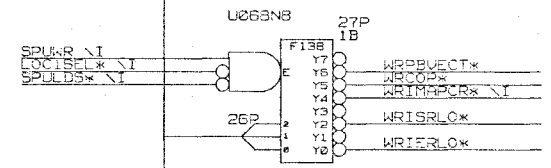
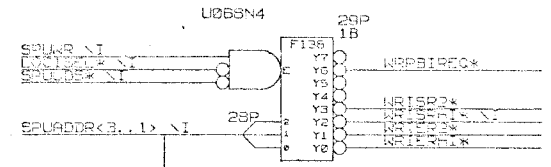
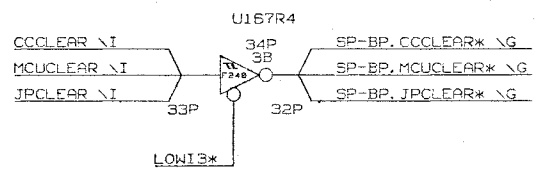
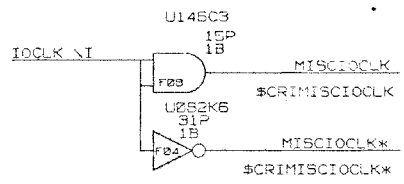
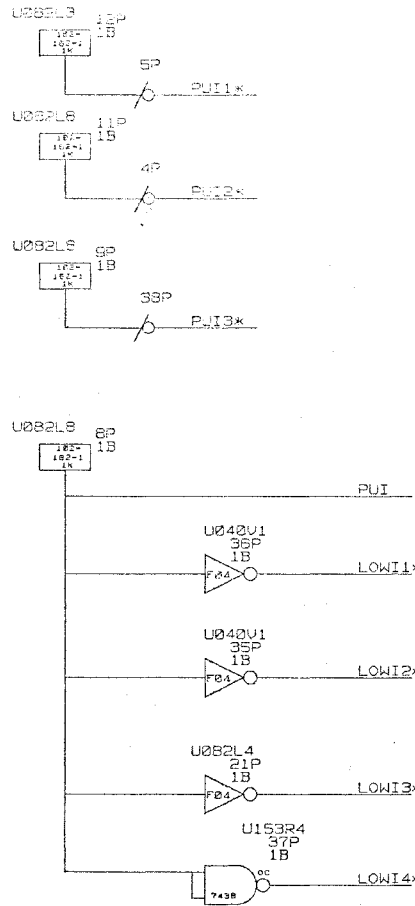


PBUS INTERRUPT RECEIVER

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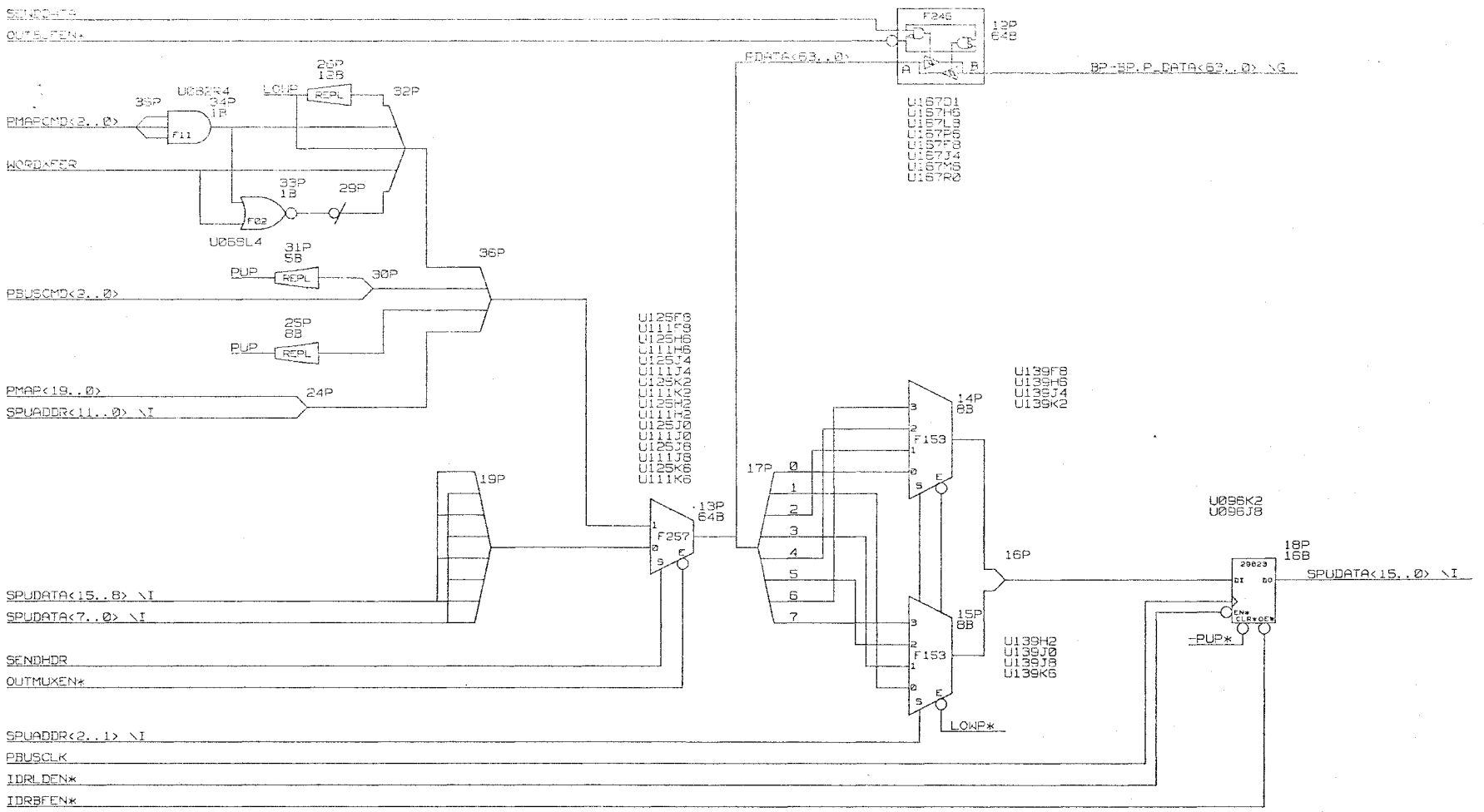
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 REVISID: Mon Sep 10 17:13:19 1984 | PAGE: SPU.2 IO.10
 ABBR: IO
 ENGR: NOBLES



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TITLE: IO	ABBR: IO
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Mon Sep 10 17:17:21 1984	PAGE: SPU.2 IO.11



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DEFINE
 PUP
 STEPASSIVE

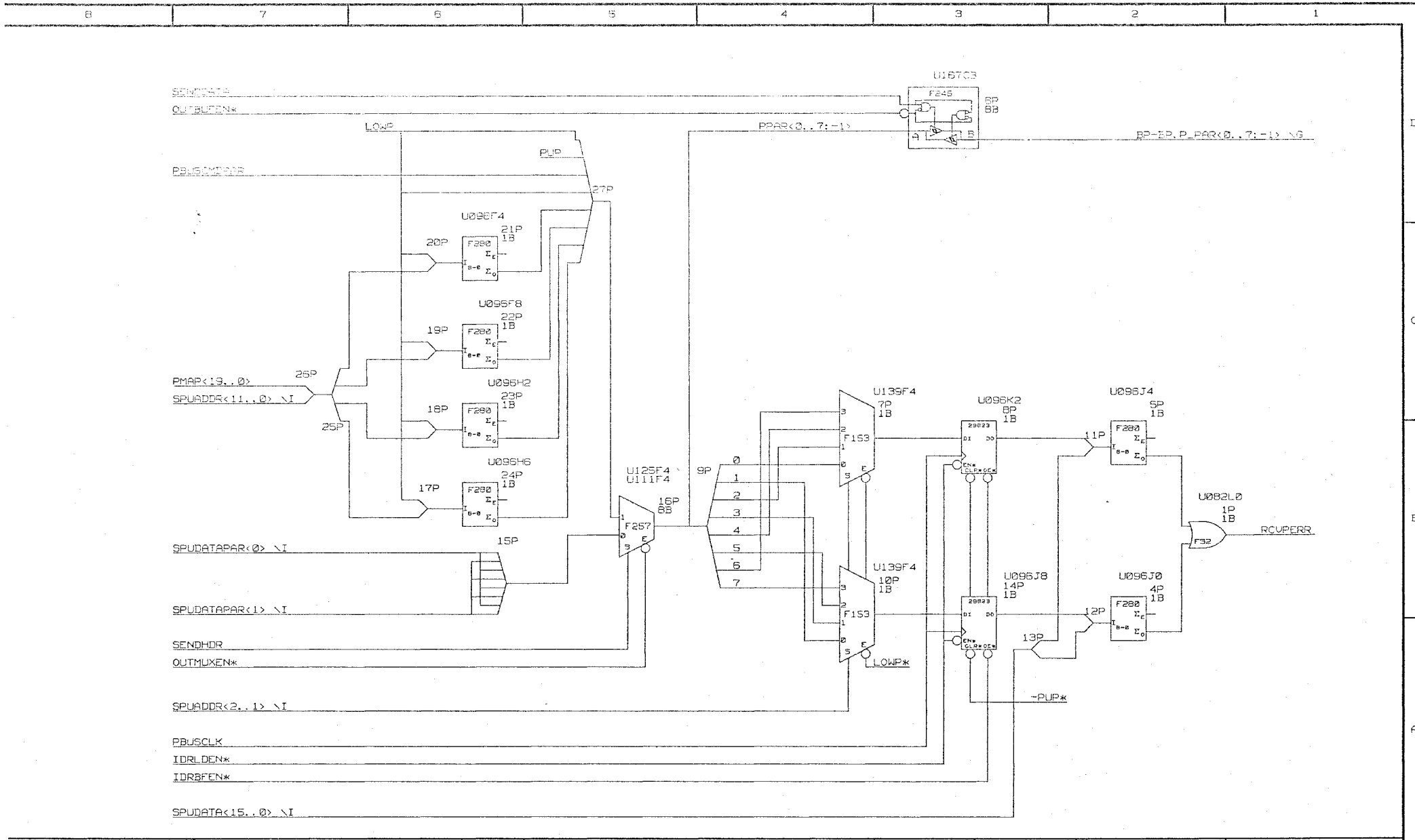


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 DRAWING: 410-00131-300 D01

ABBR: PBUS
 ENGR: NOBLES

REVISED: Fri Sep 14 11:10:40 1984

PAGE: SPU.2 PBUS.1



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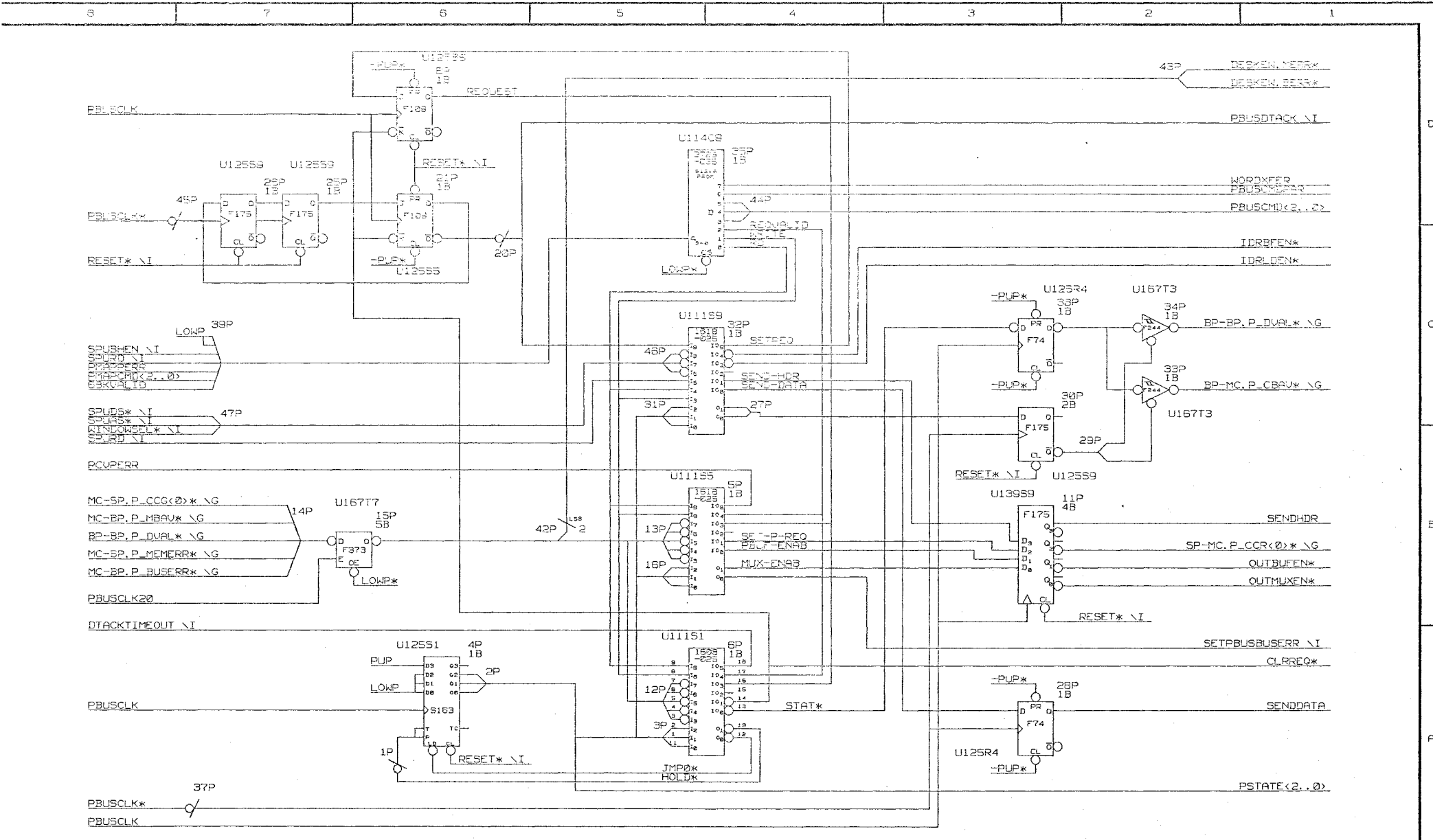


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DRAWING: 410-000131-300 D01

ABBR: PBUS
ENGR: NOBLES

REVISED: Fri Sep 14 11:11:23 1984

PAGE: SPU.2 PBUS.2



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TITLE: PBUS (STATE MACHINE)

DRAWING: 410-000131-300 D08

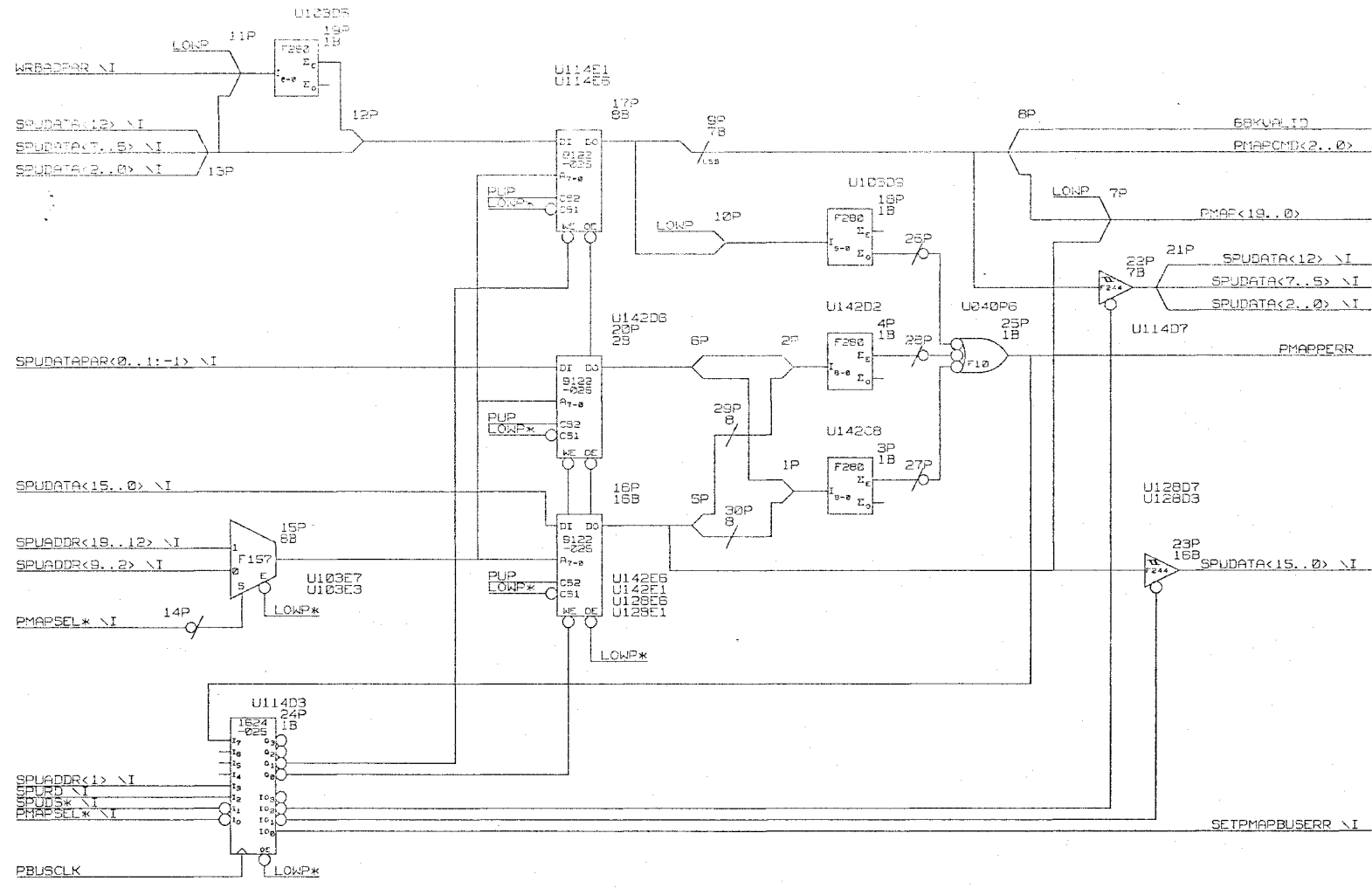
REVISED: Thu Jan 3 09:35:32 1985

ABBR: PBUS

ENGR: NOBLE.S

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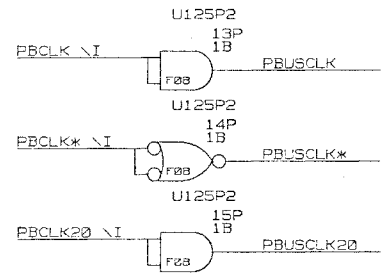
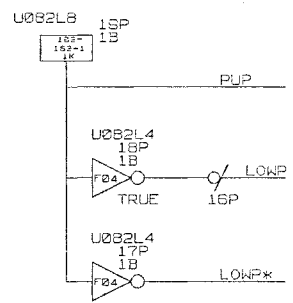
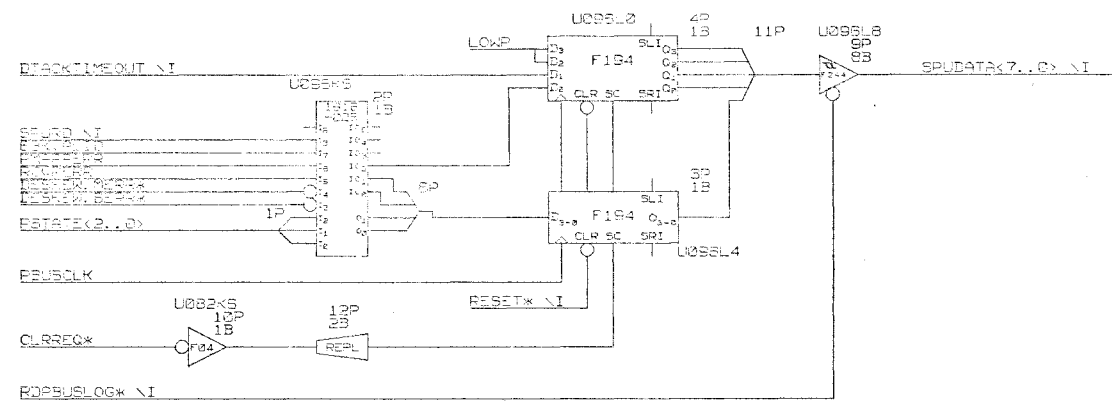
SPU.2 PBUS.3



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TITLE: PBUS (PBUS MAP)	ABBR: PBUS
DRAWING: 410-00131-300 D01	ENGR: NOBLES
REVISED: Fri Sep 14 11:13:46 1984	PAGE: SPU.2 PBUS.4

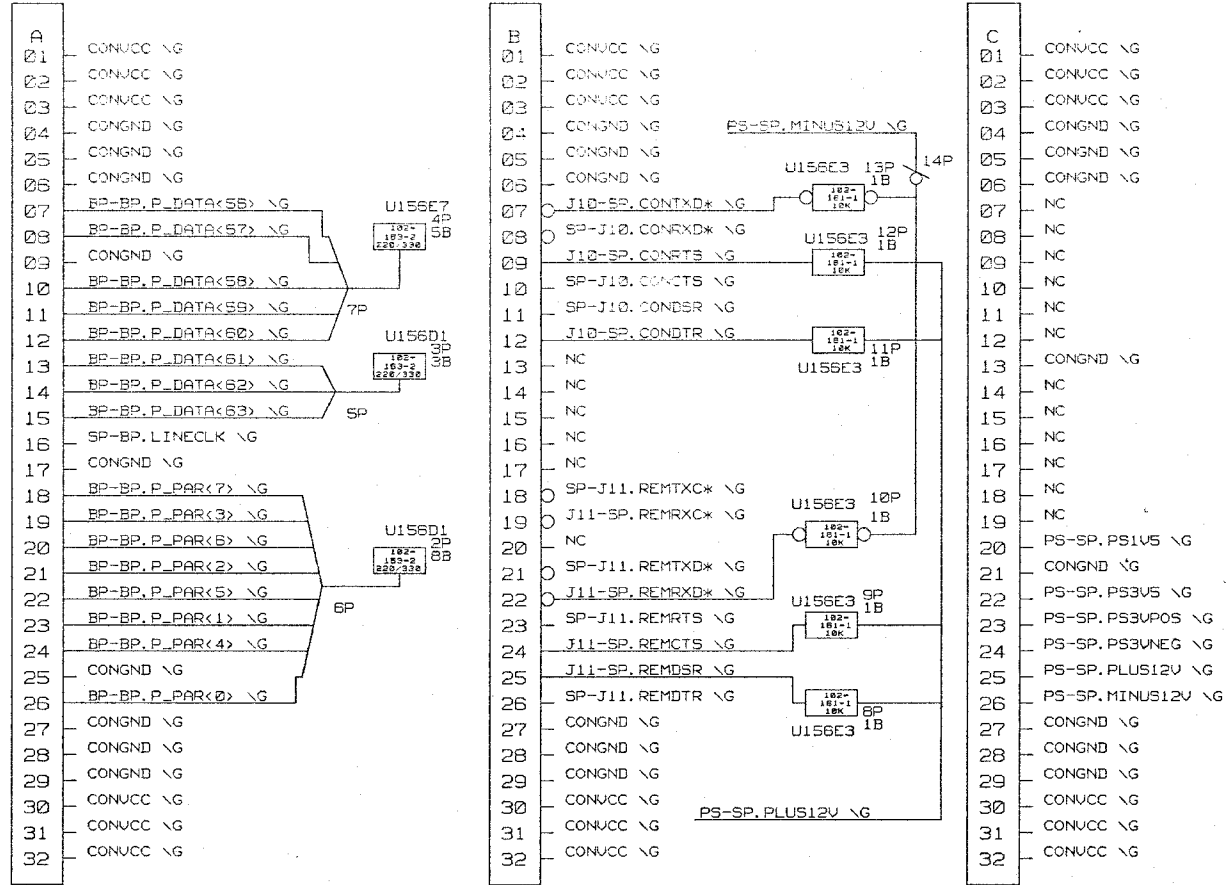


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TITLE: PBUS (PBUS ERROR LOG)	ABBR: PBUS
DRAWING: 410-020131-300 D03	ENGR: NOBLES
REVISED: Mon Jan 7 17:05:46 1985	PAGE: SPU. 2 PBUS. 5

1P
300-41512-595
U15609



PBUS

SERIAL LINES

PWR SUPPLIES

(CONNECTOR P1)

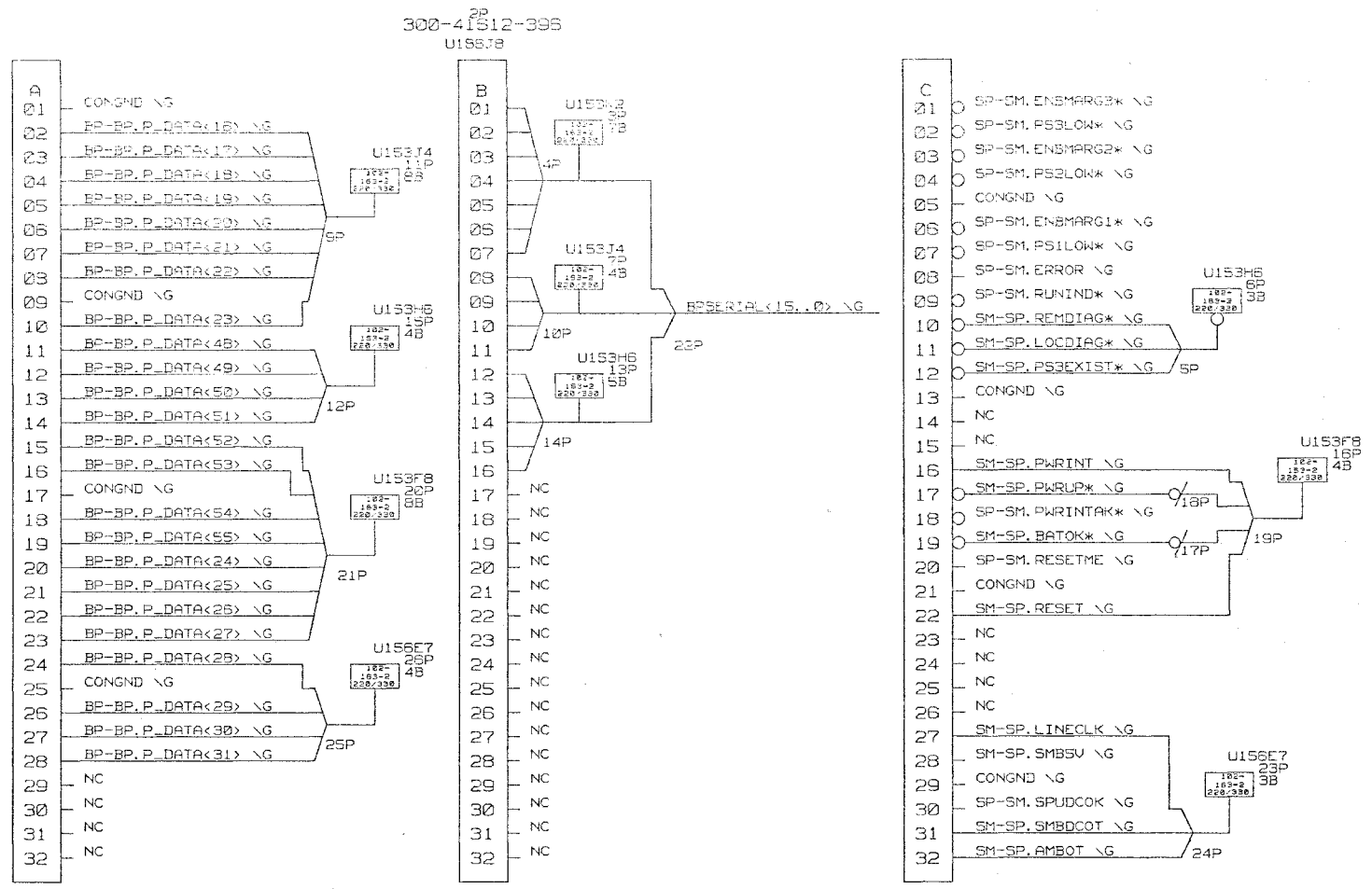
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DEFINE
X.FIRST4
X.STEP=512



TITLE: SPUCON
DRAWING: 410-000131-300 D01
REVISID: Fri Sep 14 11:16:22 1984
PAGE: SPU.2 SPUCON.1

ABBR: SPUCON
ENGR: NOBLES



PBUS

SERIAL #

SMB

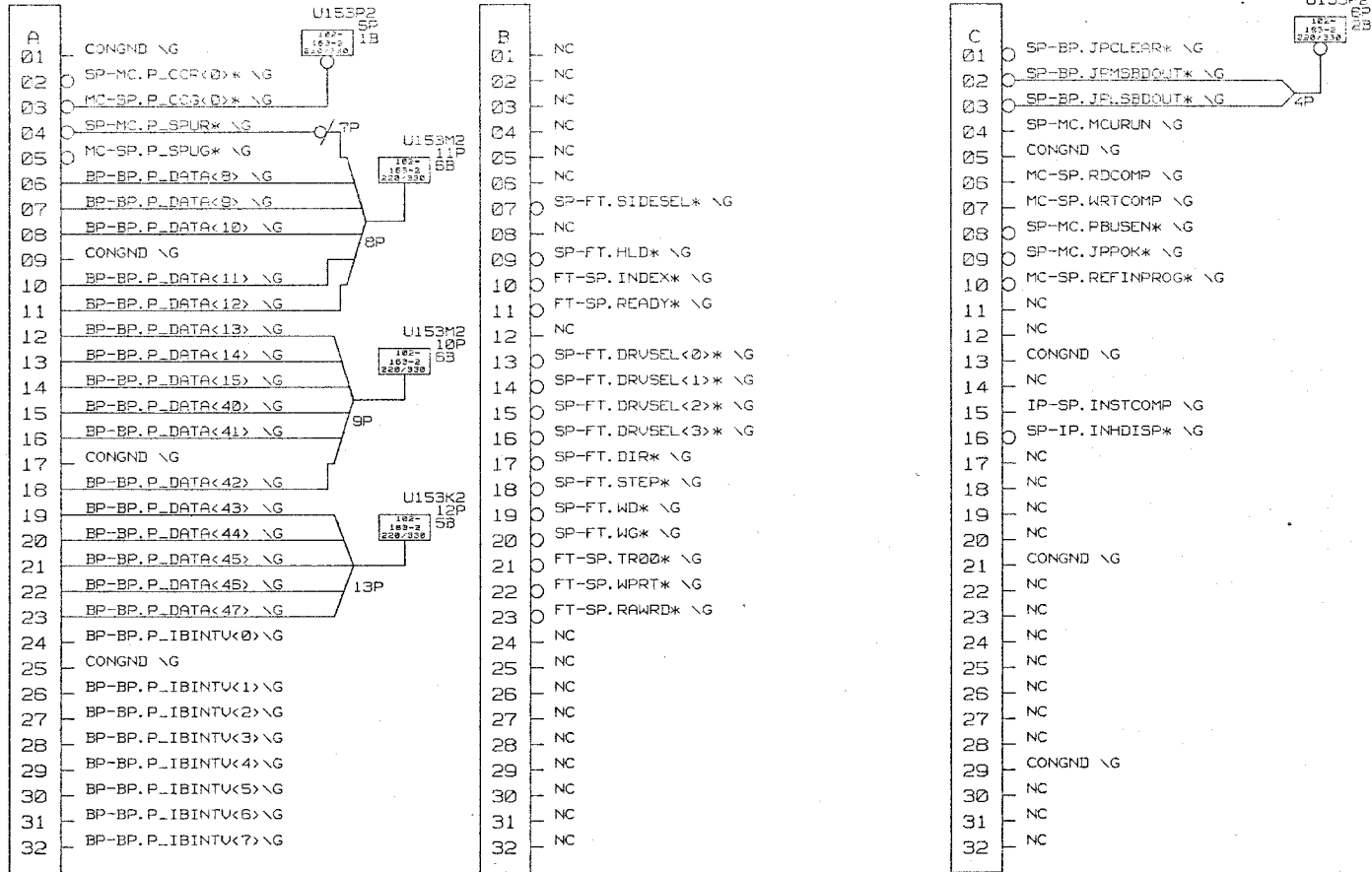
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TITLE: SPUCON
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 ENGR: NOBLES
 REVISED: Fri Sep 14 11:17:20 1984
 PAGE: SPU, 2 SPUCON, 2

3P
300-41512-395
U189N7



PBUS

FLOPPY TAPE

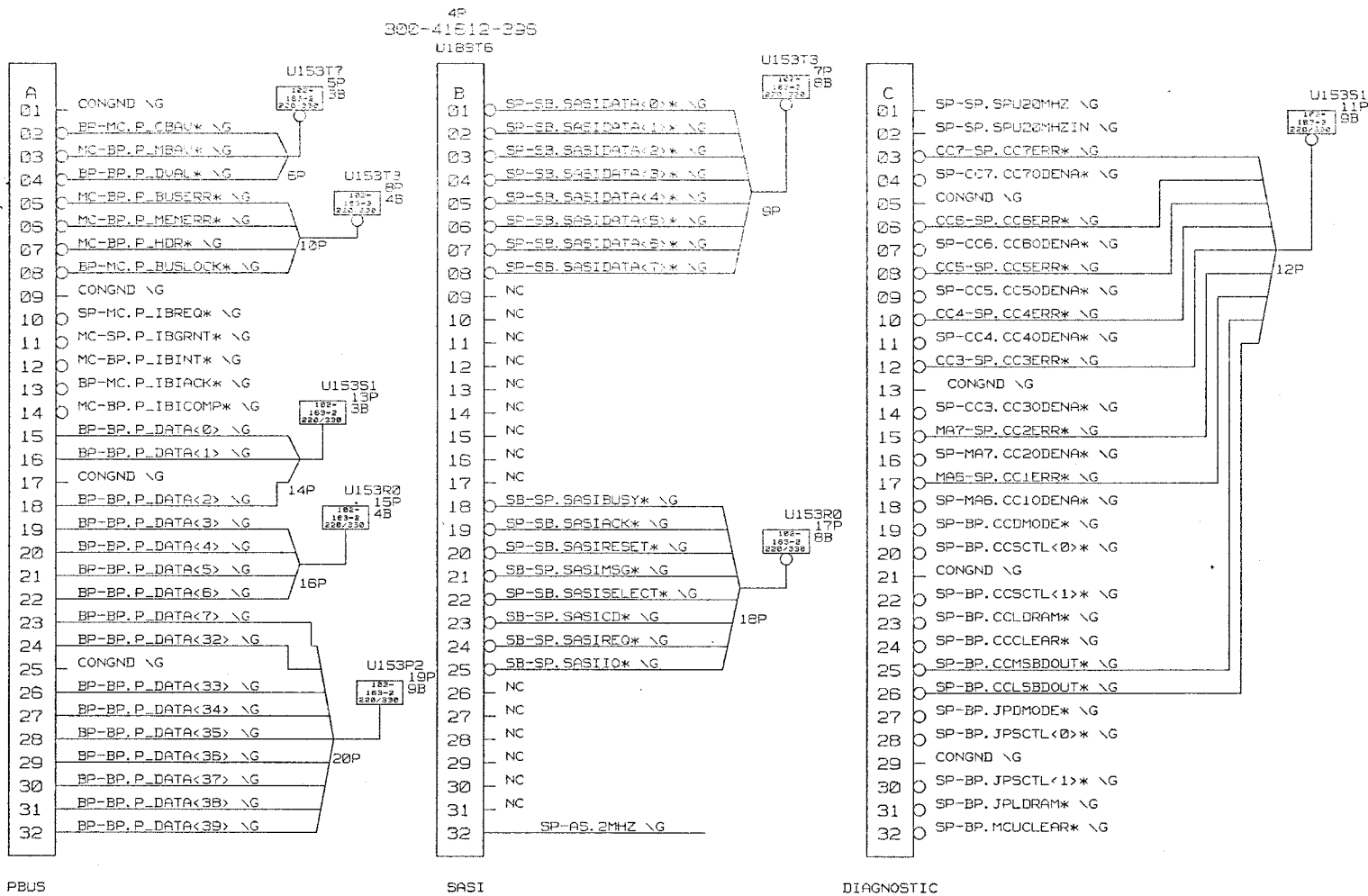
DIAGNOSTIC

(CONNECTOR P3)

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TITLE: SPUCON	ABBR: SPUCON
DRAWING: 410-000131-300 D01	ENGR: NOBLES
REVISED: Fri Sep 14 11:19:51 1984	PAGE: SPU.2 SPUCON.4

5P
300-41612-396
U163Y5

A	01	CONVCC \G
	02	CONVCC \G
	03	CONVCC \G
	04	CONGND \G
	05	CONGND \G
	06	CONGND \G
	07	SP-IP, IPU20MHZ \G
	08	SP-IP, IPUMPHASE \G
	09	CONGND \G
	10	SP-AT, ATU20MHZ \G
	11	SP-AT, ATUMPHASE \G
	12	SP-PC, PCU20MHZ \G
	13	SP-PC, PCUMPHASE \G
	14	SP-MC, MCU20MHZ \G
	15	SP-MC, MCUMPHASE \G
	16	SP-MC, MUCGPHASE \G
	17	CONGND \G
	18	SP-IP, IPUODENA* \G
	19	IP-SP, IPUERR* \G
	20	SP-AT, ATUODENA* \G
	21	AT-SP, ATUERR* \G
	22	SP-PC, PCUODENA* \G
	23	PC-SP, PCUERR* \G
	24	SP-MC, MCUODENA* \G
	25	CONGND \G
	26	MC-SP, MUCUERR* \G
	27	CONGND \G
	28	CONGND \G
	29	CONGND \G
	30	CONVCC \G
	31	CONVCC \G
	32	CONVCC \G

B	01	CONVCC \G
	02	CONVCC \G
	03	CONVCC \G
	04	CONGND \G
	05	CONGND \G
	06	CONGND \G
	07	SP-CC5, CC520MHZ \G
	08	SP-CC5, CC5MPHASE \G
	09	SP-CC5, CC5GPHASE \G
	10	SP-CC6, CC620MHZ \G
	11	SP-CC6, CC6MPHASE \G
	12	SP-CC6, CC6GPHASE \G
	13	SP-CC7, CC720MHZ \G
	14	SP-CC7, CC7MPHASE \G
	15	SP-CC7, CC7GPHASE \G
	16	SP-CC4, CC4GPHASE \G
	17	SP-CC4, CC4MPHASE \G
	18	SP-CC4, CC420MHZ \G
	19	SP-CC3, CC3GPHASE \G
	20	SP-CC3, CC3MPHASE \G
	21	SP-CC3, CC320MHZ \G
	22	SP-MA7, CC2GPHASE \G
	23	SP-MA7, CC2MPHASE \G
	24	SP-MA7, CC220MHZ \G
	25	SP-MA6, CC1GPHASE \G
	26	SP-MA6, CC1MPHASE \G
	27	CONGND \G
	28	CONGND \G
	29	CONGND \G
	30	CONVCC \G
	31	CONVCC \G
	32	CONVCC \G

C	01	CONVCC \G
	02	CONVCC \G
	03	CONVCC \G
	04	CONGND \G
	05	CONGND \G
	06	CONGND \G
	07	SP-AS, ASUMPHASE \G
	08	SP-AS, ASU20MHZ \G
	09	SP-VC, VCUMPHASE \G
	10	SP-VC, VCU20MHZ \G
	11	SP-VP0, VPU0MPHASE \G
	12	SP-VP1, VPU120MHZ \G
	13	CONGND \G
	14	SP-VP1, VPU1MPHASE \G
	15	SP-VP0, VPU020MHZ \G
	16	AS-SP, ASUERR* \G
	17	SP-AS, ASUODENA* \G
	18	VC-SP, VCUERR* \G
	19	SP-VC, VCUODENA* \G
	20	VP1-SP, VPU1ERR* \G
	21	CONGND \G
	22	SP-VP1, VPU1ODENA* \G
	23	VP0-SP, VPU0ERR* \G
	24	SP-VP0, VPU0ODENA* \G
	25	MC-SP, SOUTERR* \G
	26	SP-MA6, CC120MHZ \G
	27	CONGND \G
	28	CONGND \G
	29	CONGND \G
	30	CONVCC \G
	31	CONVCC \G
	32	CONVCC \G

U153T7
7D
4B

U153T7
6C
5B

DIAGNOSTIC

DIAGNOSTIC

DIAGNOSTIC

(CONNECTOR P5)

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DRAWING: 410-020131-300 D01
REVISED: Fri Sep 14 11:20:42 1984

ABBR: SPUCON
ENGR: NOBLES

PAGE: SPU.2 SPUCON.5